Dual 12-/14-/16-Bit, 1 GSPS, Digital-to-Analog Converters

AD9776A/AD9778A/AD9779A

FEATURES

Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions
SFDR = 78 dBc to f_{OUT} = 100 MHz
Single carrier WCDMA ACLR = 79 dBc @ 80 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth
Auxiliary DACs allow control of external VGA and offset control
Multiple chip synchronization interface
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
100-lead, exposed paddle TQFP

APPLICATIONS

Wireless infrastructure
WCDMA, CDMA2000, TD-SCDMA, WiMax, GSM
Digital high or low IF synthesis
Internal digital upconversion capability
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9776A/AD9778A/AD9779A are dual, 12-/14-/16-bit, high dynamic range, digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting a multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the ADL537x FMOD series from Analog Devices, Inc. A serial peripheral interface (SPI) provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 µm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in a 100-lead TQFP.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs are easily configured for various single-ended or differential circuit topologies.
4. CMOS data input interface with adjustable set up and hold.
5. Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth.

TYPICAL SIGNAL CHAIN

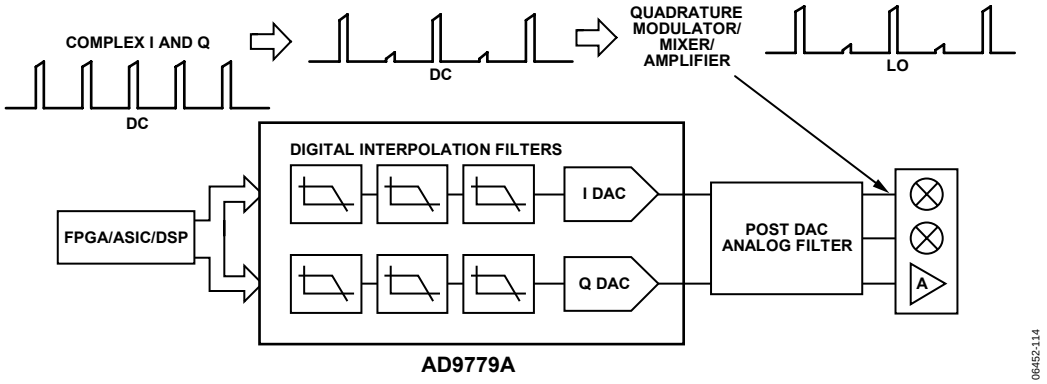

Figure 1.

Rev. 0

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REVISION HISTORY

8/07—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

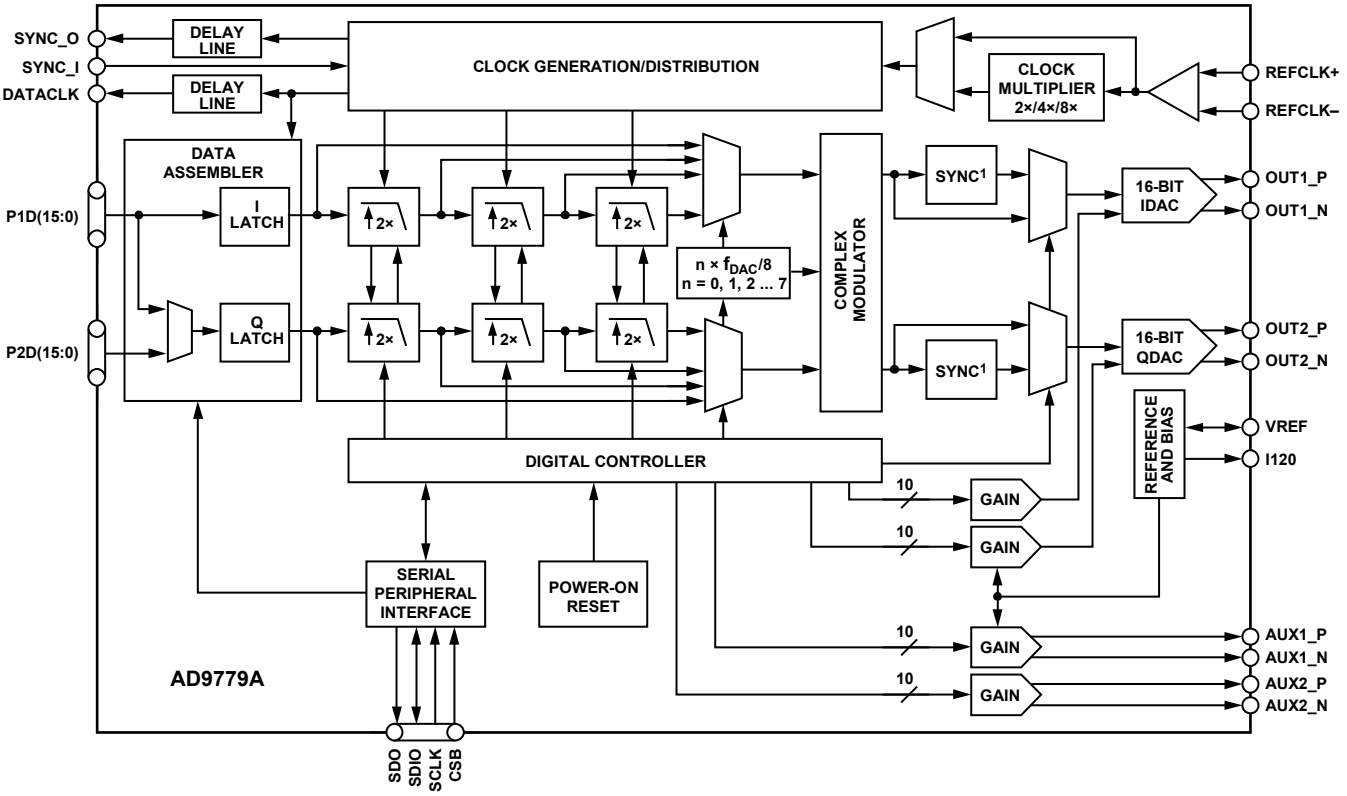

Figure 2. AD9776A/AD9778A/AD9779A Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9776A			AD9778A			AD9779A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.1			±0.65			±2.1		LSB
Integral Nonlinearity (INL)		±0.6			±1			±3.7		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current[1]	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
AUX DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	2.05	1.70	1.8	2.05	1.70	1.8	2.05	V
POWER CONSUMPTION										
1× Mode, f_{DAC} = 100 MSPS, IF = 1 MHz		250	300		250	300		250	300	mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL Off		498			498			498		mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL On		588			588			588		mW
4× Mode, $f_{DAC}/4$ Modulation, f_{DAC} = 500 MSPS, IF = 137.5 MHz, Q DAC Off		572			572			572		mW
8× Mode, $f_{DAC}/4$ Modulation, f_{DAC} = 1 GSPS, IF = 262.5 MHz		980			980			980		mW
Power-Down Mode		2.5	9.8		2.5	9.8		2.5	9.8	mW
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
Maximum Input Data Rate at Interpolation					
1×		300			MSPS
2×		250			MSPS
4×		200			MSPS
8×	DVDD18, CVDD18 = 1.8 V ± 5%	112.5			MSPS
8×	DVDD18, CVDD18 = 1.9 V ± 5%	125			MSPS
8×	DVDD18, CVDD18 = 2.0 V ± 2%	137.5			MSPS
CMOS OUTPUT LOGIC LEVEL (DATACLK, PIN 37)[1]					
Output V_{OUT} Logic High		2.4			V
Output V_{OUT} Logic Low				0.4	V
LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I–)	SYNC_I+ = V_{IA}, SYNC_I– = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate				125	MSPS
Set-Up Time, SYNC_I to DAC Clock		0.3			ns
Hold Time, SYNC_I to DAC Clock		0.9			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O–)	SYNC_O+ = V_{OA}, SYNC_O– = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}				1375	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, R_O	Single-ended	80	100	120	Ω
Maximum Clock Rate	DVDD18, CVDD18 = 1.8 V ± 5%	0.9			GHz
	DVDD18, CVDD18 = 1.9 V ± 5%	1.0			GHz
	DVDD18, CVDD18 = 2.0 V ± 2%	1.1			GHz
DAC CLOCK INPUT (REFCLK+, REFCLK–)					
Differential Peak-to-Peak Voltage		400	800	2000	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate		1			GSPS
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High				12.5	ns
Minimum Pulse Width Low				12.5	ns
Set-Up Time, SDI to SCLK		1.6			ns
Hold Time, SDI to SCLK		0.0			ns
Data Valid, SDO to SCLK		2.0			ns

[1] Specification is at a DATACLK frequency of 100 MHz into a 1 kΩ load, maximum drive capability of 8 mA. At higher speeds or greater loads, best practice suggests using an external buffer for this signal.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
INPUT DATA (ALL MODES, –40°C to +85°C)[1]				
Setup Time, Input Data to DATACLK	3.0			ns
Hold Time, Input Data to DATACLK	–0.05			ns
Setup Time, Input Data to REFCLK	–0.8			ns
Hold Time, Input Data to REFCLK	3.8			ns

[1] Timing vs. temperature and data valid keep out windows are delineated in Table 20.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9776A			AD9778A			AD9779A			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		81			81			82		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		85			85			87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		87			87			91		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		80			85			85		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		75			81			81		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		75			80			81		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING										
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		–152			–155			–158		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		–155			–159			–160		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		–157.5			–160			–161		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		76			78			79		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		69			73			74		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		77.5			80			81		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		76			78			78		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD33, DVDD33	AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD18, CVDD18	AGND, DGND, CGND	−0.3 V to +2.1 V
AGND	DGND, CGND	−0.3 V to +0.3 V
DGND	AGND, CGND	−0.3 V to +0.3 V
CGND	AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT	AGND	−0.3 V to AVDD33 + 0.3 V
OUT1_P, OUT1_N, OUT2_P, OUT2_N, AUX1_P, AUX1_N, AUX2_P, AUX2_N	AGND	−1.0 V to AVDD33 + 0.3 V
P1D<15> to P1D<0>, P2D<15> to P2D<0>	DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE	DGND	−0.3 V to DVDD33 + 0.3 V
REFCLK+, REFCLK−	CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

100-lead, thermally enhanced TQFP_EP package, θ_{JA} = 19.1°C/W with the bottom EPAD soldered to the PCB. With the bottom EPAD not soldered to the PCB, θ_{JA} = 27.4°C/W. θ_{JC} = 7.08°C/W. These specifications are valid with no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

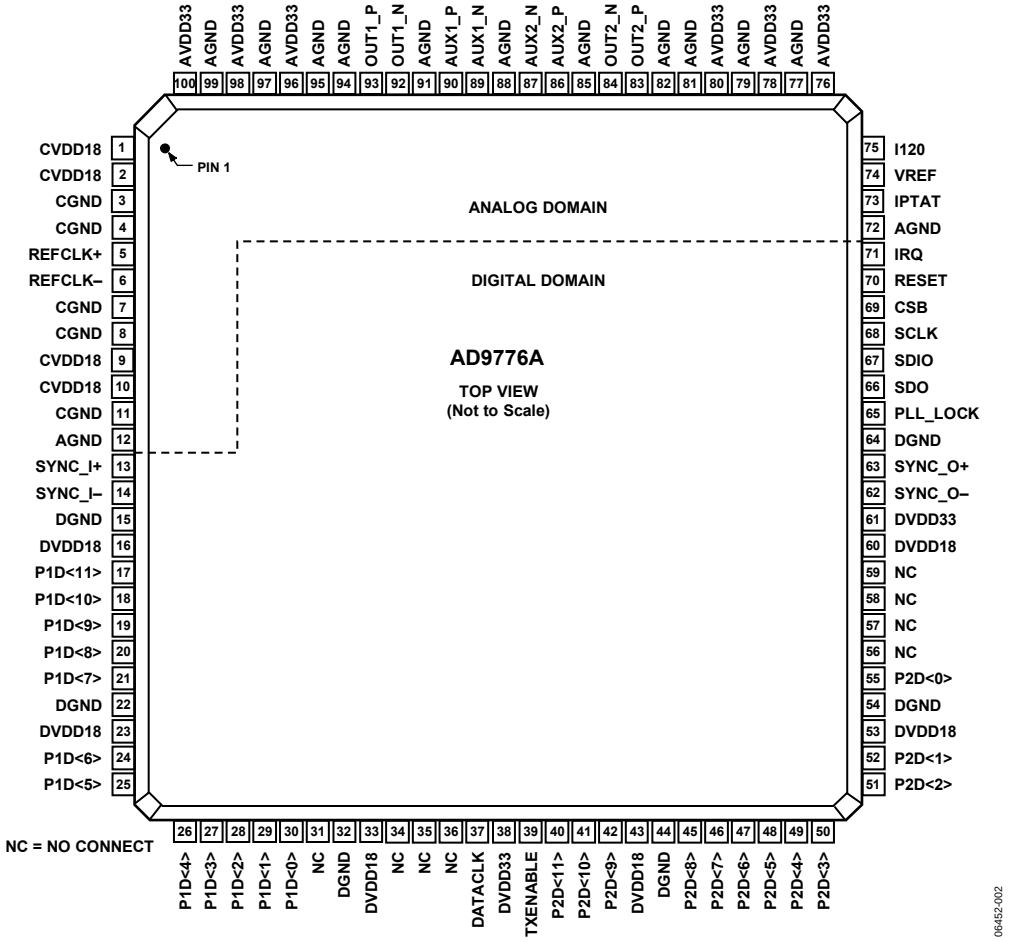

Figure 3. AD9776A Pin Configuration

Table 6. AD 9776A Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<11>	Port 1, Data Input D11 (MSB).
18	P1D<10>	Port 1, Data Input D10.
19	P1D<9>	Port 1, Data Input D9.
20	P1D<8>	Port 1, Data Input D8.
21	P1D<7>	Port 1, Data Input D7.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<6>	Port 1, Data Input D6.
25	P1D<5>	Port 1, Data Input D5.
26	P1D<4>	Port 1, Data Input D4.
27	P1D<3>	Port 1, Data Input D3.
28	P1D<2>	Port 1, Data Input D2.
29	P1D<1>	Port 1, Data Input D1.
30	P1D<0>	Port 1, Data Input D0 (LSB).
31	NC	No Connect.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	NC	No Connect.
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.

Pin No.	Mnemonic	Description
39	TXENABLE	Transmit Enable.
40	P2D<11>	Port 2, Data Input D11 (MSB).
41	P2D<10>	Port 2, Data Input D10.
42	P2D<9>	Port 2, Data Input D9.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<8>	Port 2, Data Input D8.
46	P2D<7>	Port 2, Data Input D7.
47	P2D<6>	Port 2, Data Input D6.
48	P2D<5>	Port 2, Data Input D5.
49	P2D<4>	Port 2, Data Input D4.
50	P2D<3>	Port 2, Data Input D3.
51	P2D<2>	Port 2, Data Input D2.
52	P2D<1>	Port 2, Data Input D1.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<0>	Port 2, Data Input D0 (LSB).
56	NC	No Connect.
57	NC	No Connect.
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Common.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	SPI Port Data Output.
67	SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.

Pin No.	Mnemonic	Description
72	AGND	Analog Common
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

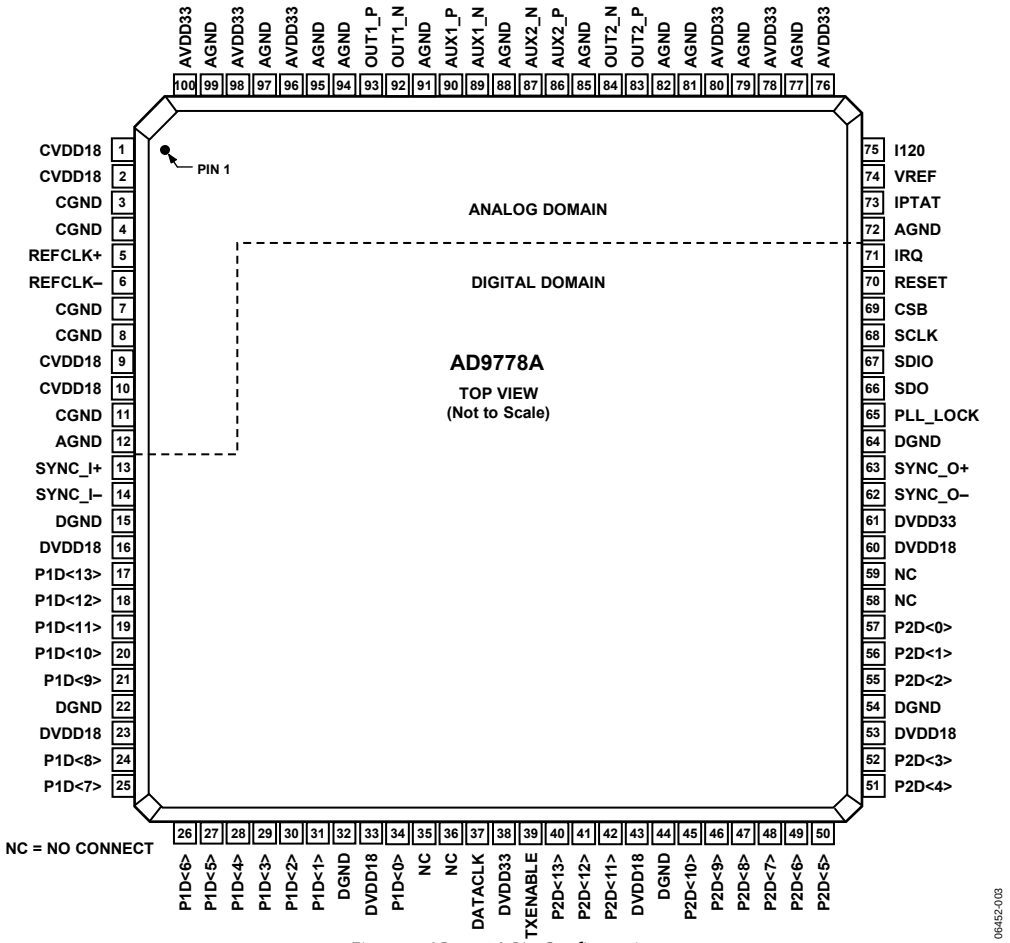

Figure 4. AD9778A Pin Configuration

Table 7. AD 9778A Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<13>	Port 1, Data Input D13 (MSB).
18	P1D<12>	Port 1, Data Input D12.
19	P1D<11>	Port 1, Data Input D11.
20	P1D<10>	Port 1, Data Input D10.
21	P1D<9>	Port 1, Data Input D9.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<8>	Port 1, Data Input D8.
25	P1D<7>	Port 1, Data Input D7.
26	P1D<6>	Port 1, Data Input D6.
27	P1D<5>	Port 1, Data Input D5.
28	P1D<4>	Port 1, Data Input D4.
29	P1D<3>	Port 1, Data Input D3.
30	P1D<2>	Port 1, Data Input D2.
31	P1D<1>	Port 1, Data Input D1.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	P1D<0>	Port 1, Data Input D0 (LSB).
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.

Pin No.	Mnemonic	Description
39	TXENABLE	Transmit Enable.
40	P2D<13>	Port 2, Data Input D13 (MSB).
41	P2D<12>	Port 2, Data Input D12.
42	P2D<11>	Port 2, Data Input D11.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<10>	Port 2, Data Input D10.
46	P2D<9>	Port 2, Data Input D9.
47	P2D<8>	Port 2, Data Input D8.
48	P2D<7>	Port 2, Data Input D7.
49	P2D<6>	Port 2, Data Input D6.
50	P2D<5>	Port 2, Data Input D5.
51	P2D<4>	Port 2, Data Input D4.
52	P2D<3>	Port 2, Data Input D3.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<2>	Port 2, Data Input D2.
56	P2D<1>	Port 2, Data Input D1.
57	P2D<0>	Port 2, Data Input D0 (LSB).
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Common.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	SPI Port Data Output.
67	SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.

Pin No.	Mnemonic	Description
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74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

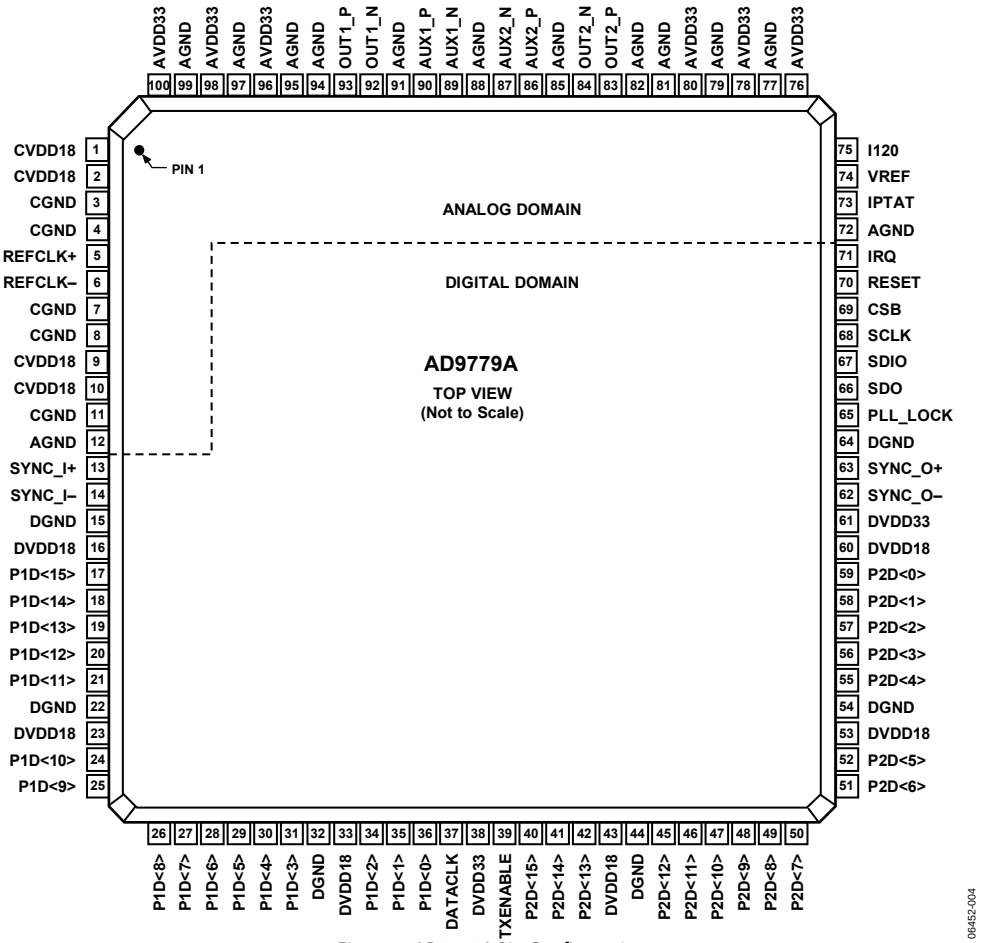


Figure 5. AD9779A Pin Configuration

Table 8. AD9779A Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	REFCLK+	Differential Clock Input.
6	REFCLK–	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<15>	Port 1, Data Input D15 (MSB).
18	P1D<14>	Port 1, Data Input D14.
19	P1D<13>	Port 1, Data Input D13.
20	P1D<12>	Port 1, Data Input D12.
21	P1D<11>	Port 1, Data Input D11.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<10>	Port 1, Data Input D10.
25	P1D<9>	Port 1, Data Input D9.
26	P1D<8>	Port 1, Data Input D8.
27	P1D<7>	Port 1, Data Input D7.
28	P1D<6>	Port 1, Data Input D6.
29	P1D<5>	Port 1, Data Input D5.
30	P1D<4>	Port 1, Data Input D4.
31	P1D<3>	Port 1, Data Input D3.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	P1D<2>	Port 1, Data Input D2.
35	P1D<1>	Port 1, Data Input D1.
36	P1D<0>	Port 1, Data Input D0 (LSB).
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D<15>	Port 2, Data Input D15 (MSB).
41	P2D<14>	Port 2, Data Input D14.
42	P2D<13>	Port 2, Data Input D13.

Pin No.	Mnemonic	Description
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<12>	Port 2, Data Input D12.
46	P2D<11>	Port 2, Data Input D11.
47	P2D<10>	Port 2, Data Input D10.
48	P2D<9>	Port 2, Data Input D9.
49	P2D<8>	Port 2, Data Input D8.
50	P2D<7>	Port 2, Data Input D7.
51	P2D<6>	Port 2, Data Input D6.
52	P2D<5>	Port 2, Data Input D5.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<4>	Port 2, Data Input D4.
56	P2D<3>	Port 2, Data Input D3.
57	P2D<2>	Port 2, Data Input D2.
58	P2D<1>	Port 2, Data Input D1.
59	P2D<0>	Port 2, Data Input D0 (LSB).
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Common.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	SPI Port Data Output.
67	SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Common.

Pin No.	Mnemonic	Description
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14 µA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 µA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

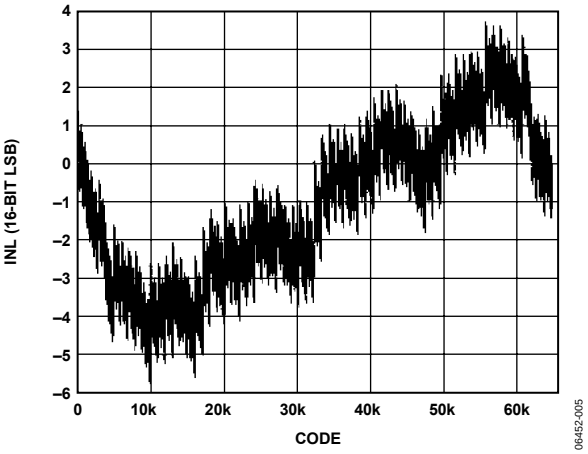


Figure 6. AD9779A Typical INL

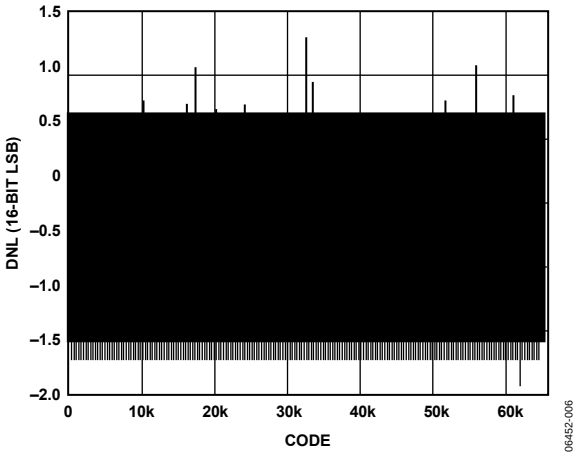


Figure 7. AD9779A Typical DNL

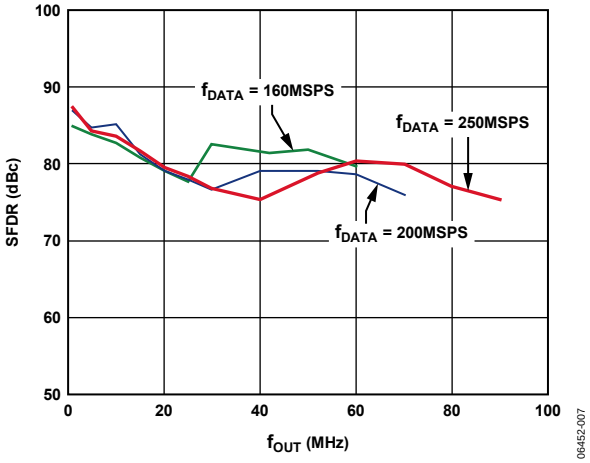


Figure 8. AD9779A In-Band SFDR vs. f_{OUT}, 1× Interpolation

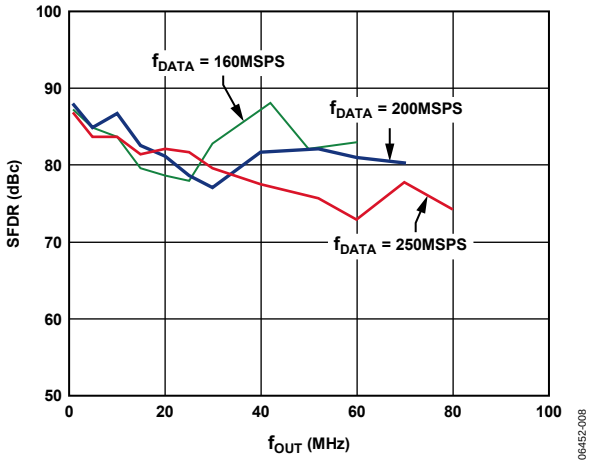


Figure 9. AD9779A In-Band SFDR vs. f_{OUT}, 2× Interpolation

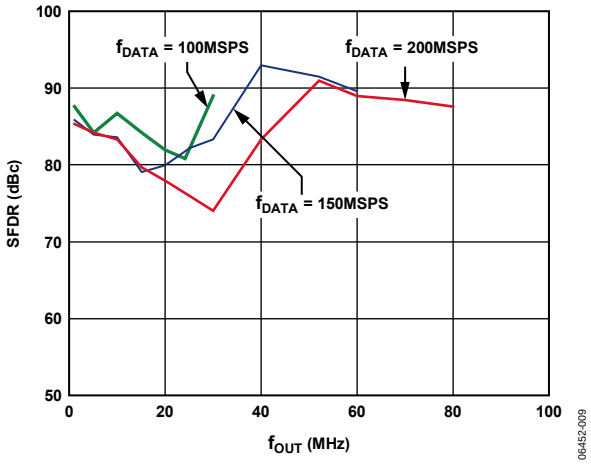


Figure 10. AD9779A In-Band SFDR vs. f_{OUT}, 4× Interpolation

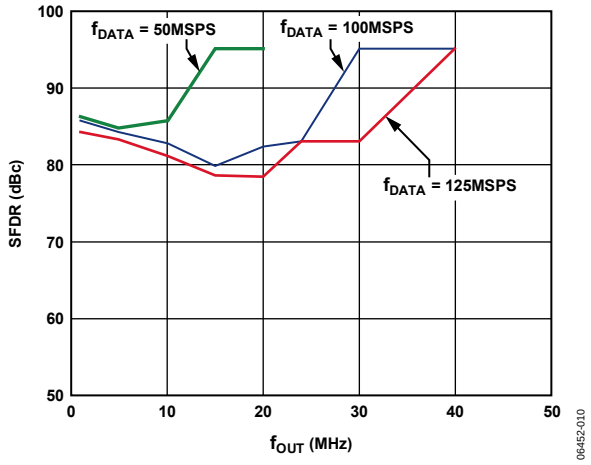


Figure 11. AD9779A In-Band SFDR vs. f_{OUT}, 8× Interpolation

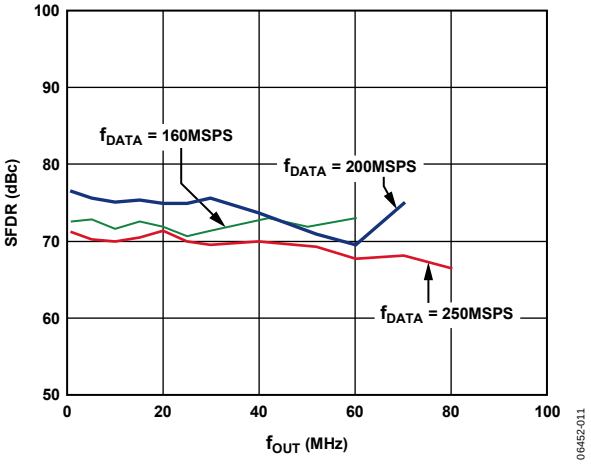


Figure 12. AD9779A Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

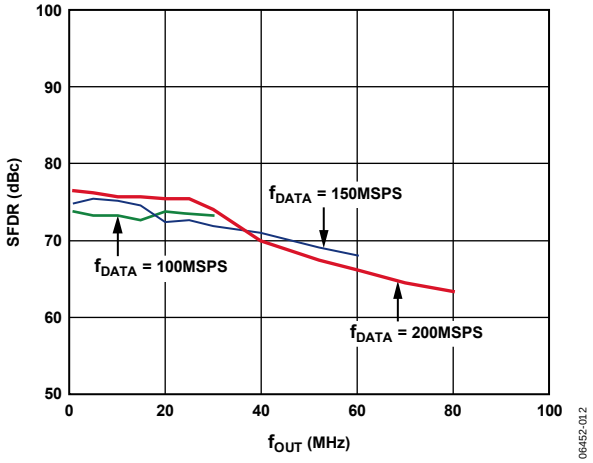


Figure 13. AD9779A Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

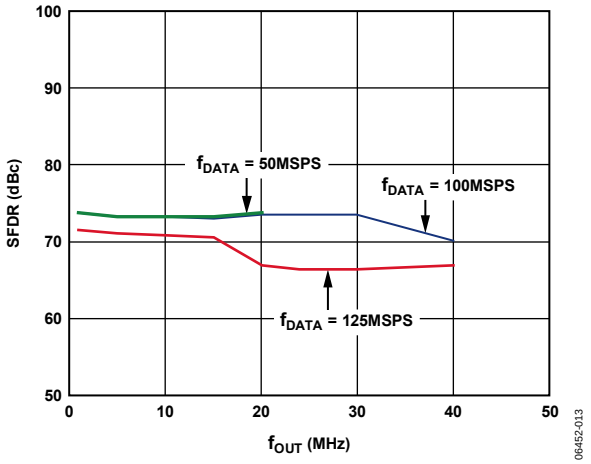


Figure 14. AD9779A Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

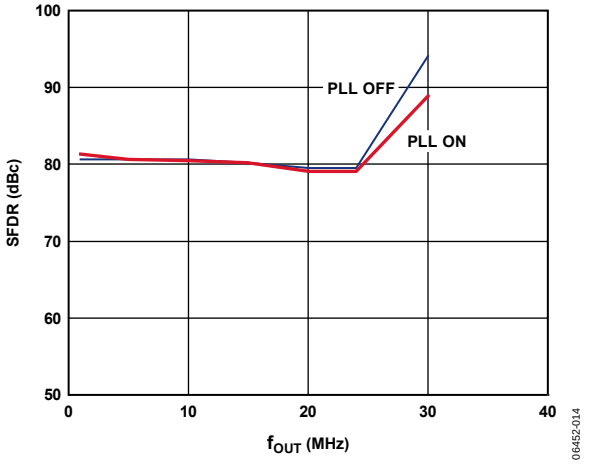


Figure 15. AD9779A In-Band SFDR, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

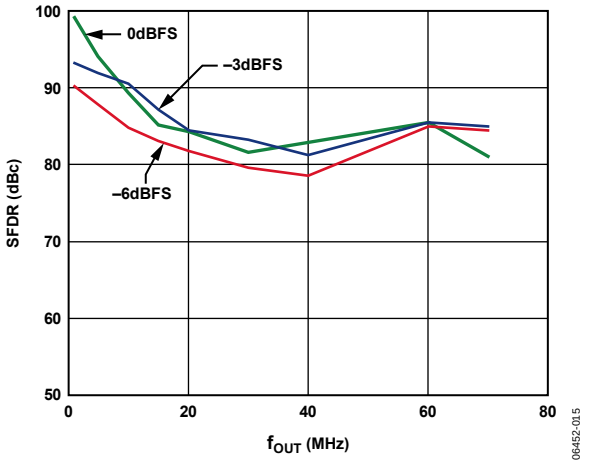


Figure 16. AD9779A In-Band SFDR vs. f_{OUT}, Digital Full-Scale

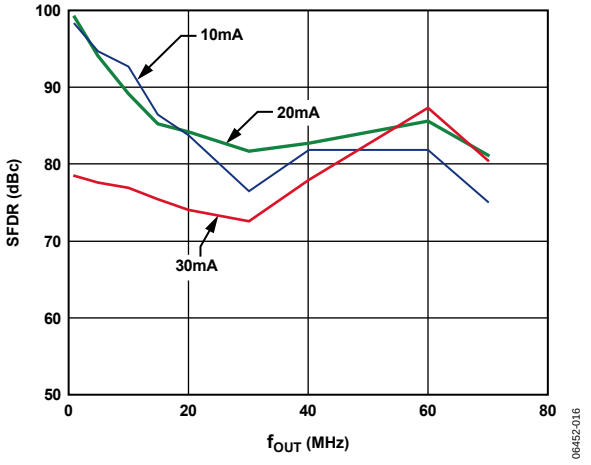


Figure 17. AD9779A In-Band SFDR vs. f_{OUT}, Output Full-Scale Current

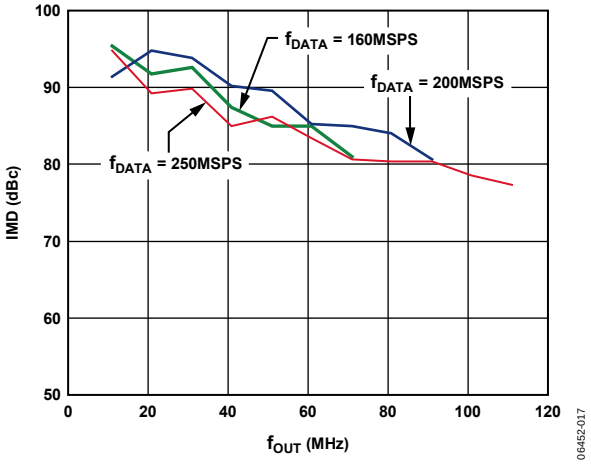


Figure 18. AD9779A Third-Order IMD vs. f_{OUT}, 1× Interpolation

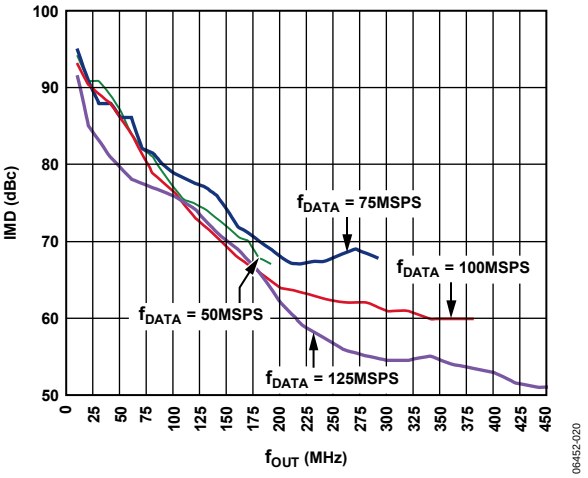


Figure 21. AD9779A Third-Order IMD vs. f_{OUT}, 8× Interpolation

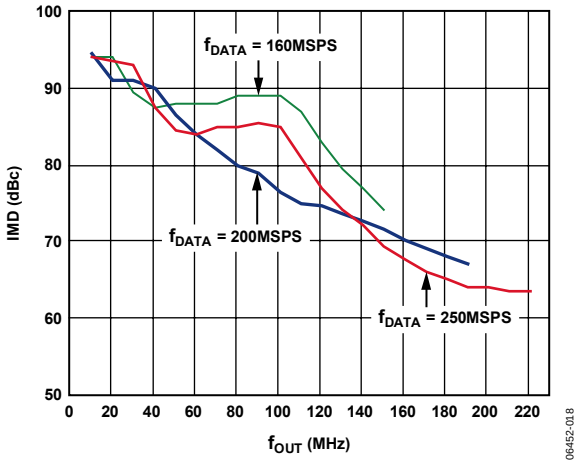


Figure 19. AD9779A Third-Order IMD vs. f_{OUT}, 2× Interpolation

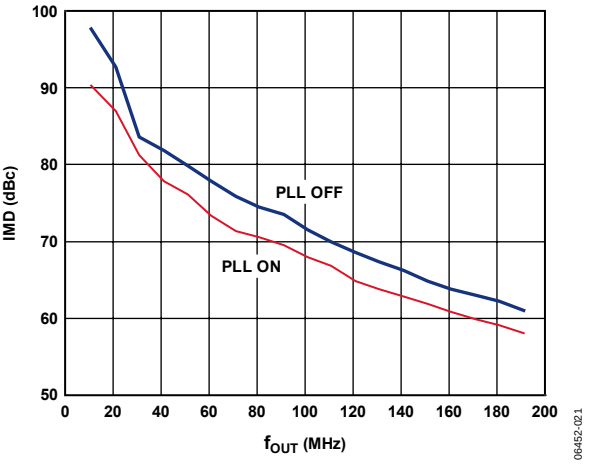


Figure 22. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On vs. PLL Off

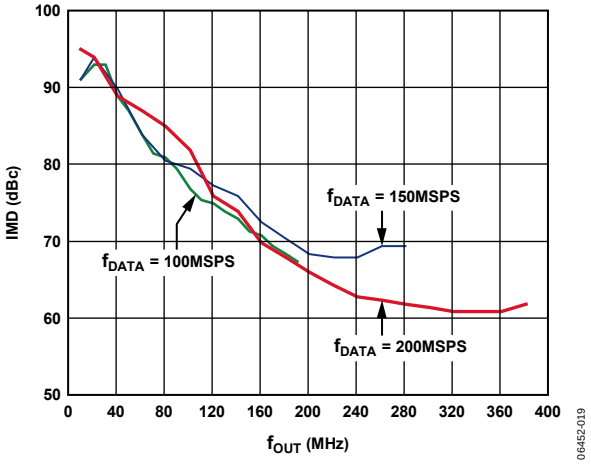


Figure 20. AD9779A Third-Order IMD vs. f_{OUT}, 4× Interpolation

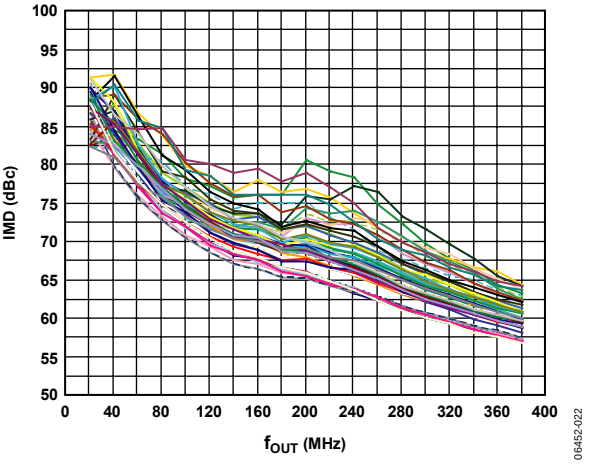


Figure 23. AD9779A Third-Order IMD vs. f_{OUT}, over 50 Parts, 4× Interpolation, f_{DATA} = 200 MSPS

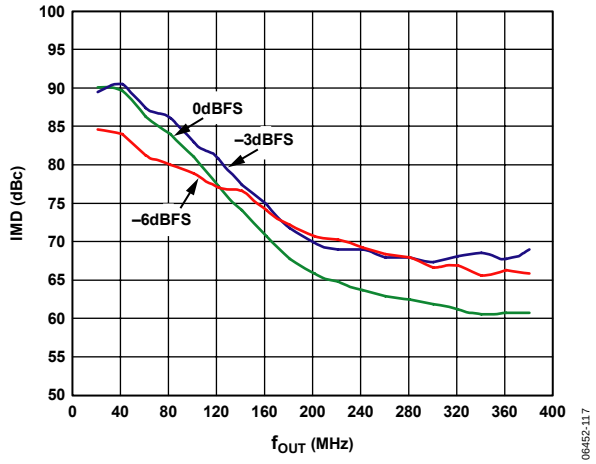


Figure 24. AD9779A IMD Performance vs. Digital Full-Scale Input over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

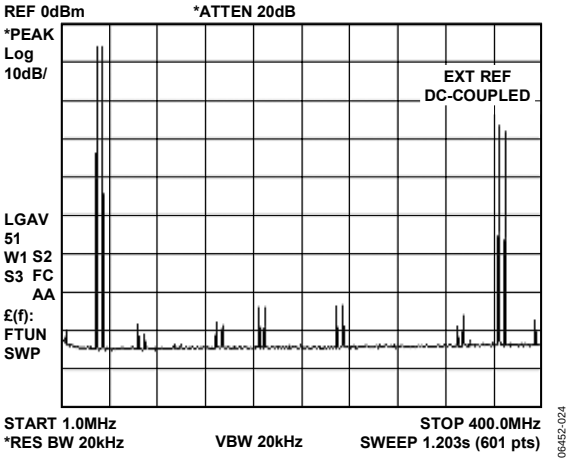


Figure 27. AD9779A Two-Tone Spectrum, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz, 35 MHz

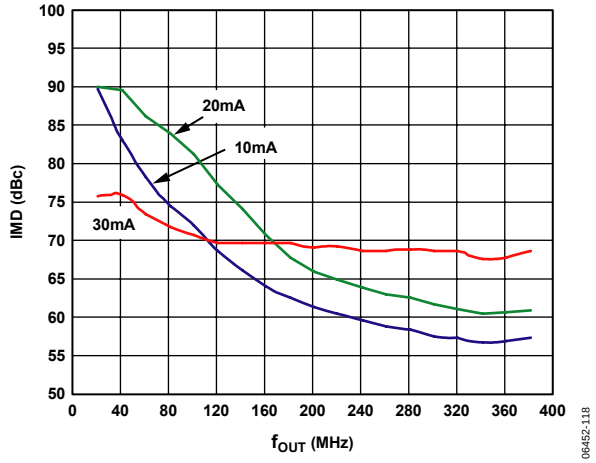


Figure 25. AD9779A IMD Performance vs. Full-Scale Output Current over Output Frequency, 4× Interpolation, f_{DATA} = 200 MSPS

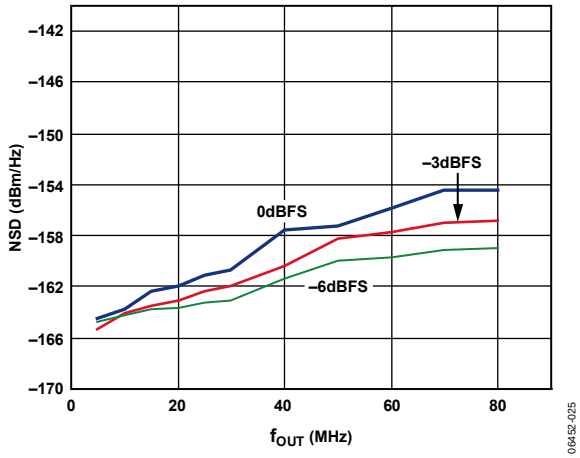


Figure 28. AD9779A Noise Spectral Density vs. Digital Full-Scale over Output Frequency of Single-Tone Input, f_{DATA} = 200 MSPS, 2× Interpolation

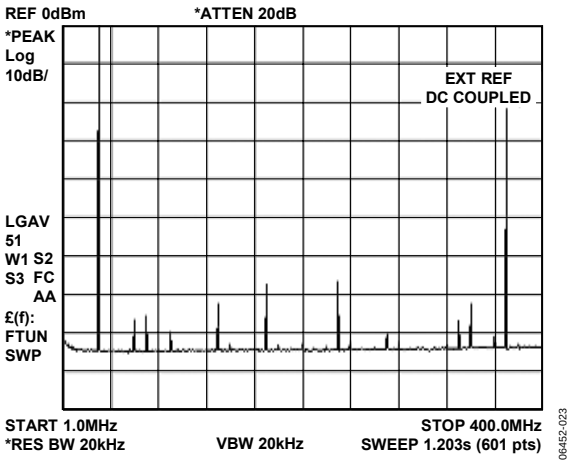


Figure 26. AD9779A Single Tone, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz

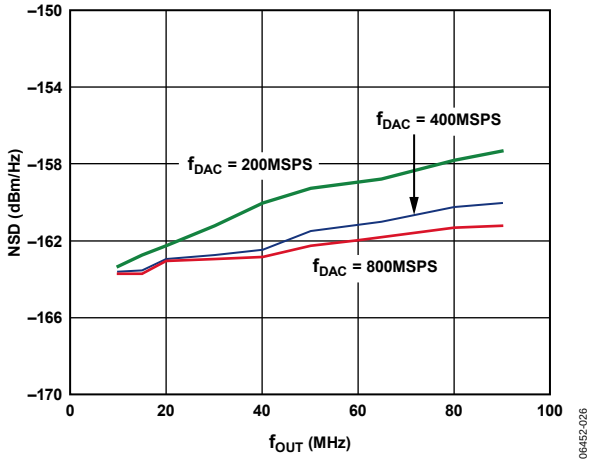


Figure 29. AD9779A Noise Spectral Density vs. f_{DAC} over Output Frequency for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

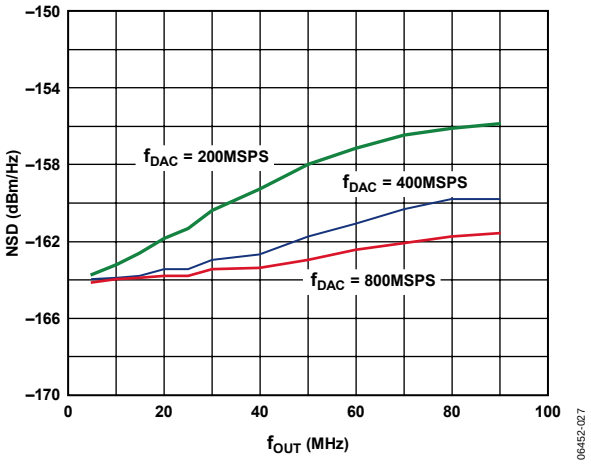


Figure 30. AD9779A Noise Spectral Density vs. f_{DAC} over Output Frequency with a Single-Tone Input at −6 dBFS

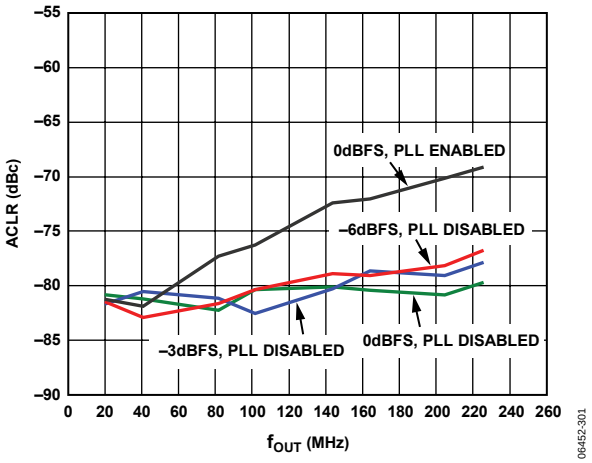


Figure 32. AD9779A ACLR for Second Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS; On-Chip Modulation Translates Baseband Signal to IF

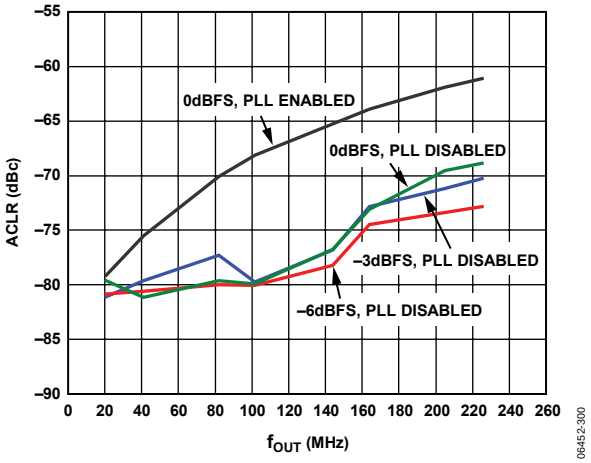


Figure 31. AD9779A ACLR for First Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

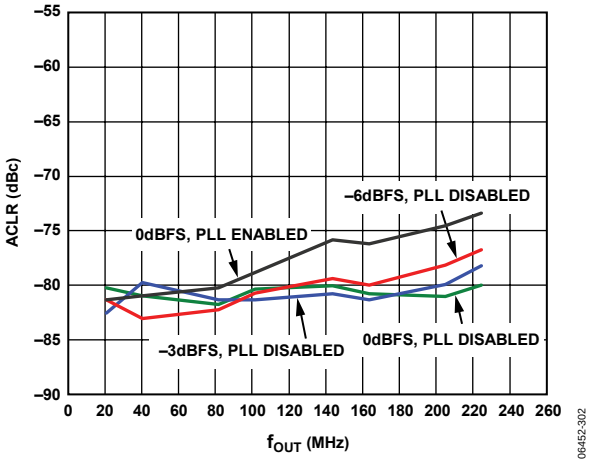


Figure 33. AD9779A ACLR for Third Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

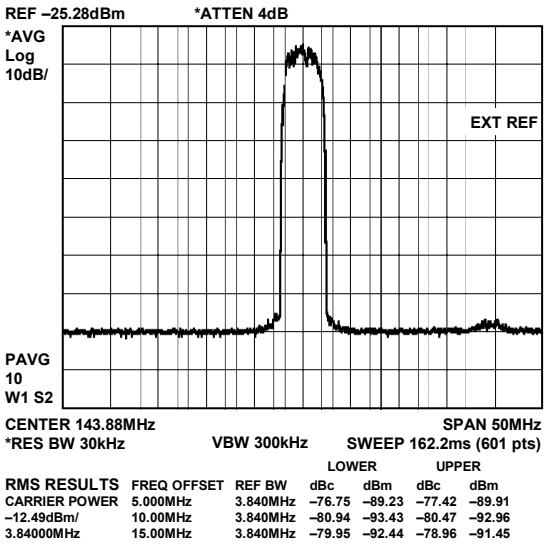


Figure 34. AD9779A WCDMA Signal, 4× Interpolation, f_{DATA} = 122.88 MSPS, f_{DAC}/4 Modulation

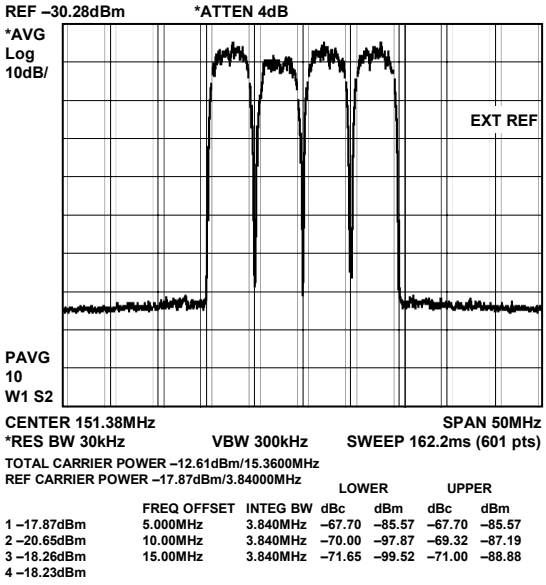


Figure 35. AD9779A Multicarrier WCDMA Signal, 4× Interpolation, f_{DAC} = 122.88 MSPS, f_{DAC}/4 Modulation

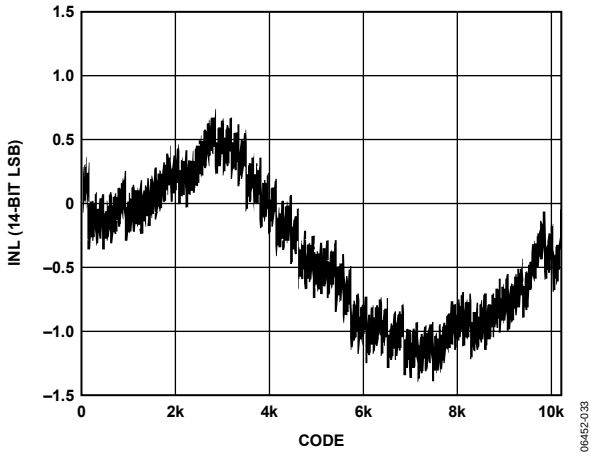


Figure 36. AD9778A Typical INL

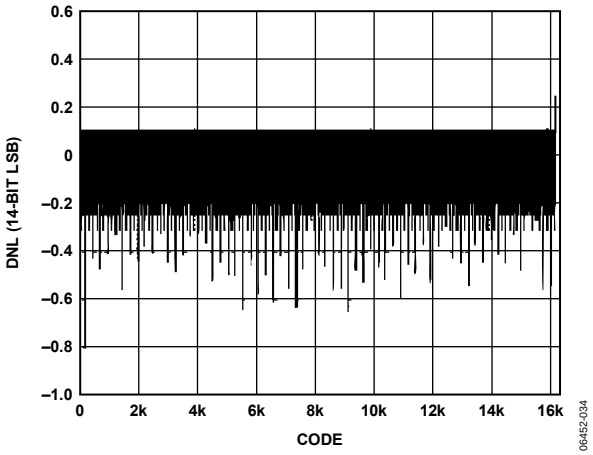


Figure 37. AD9778A Typical DNL

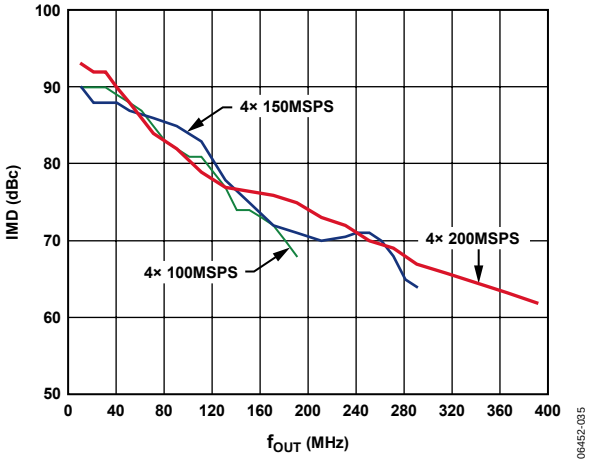


Figure 38. AD9778A IMD vs. f_{OUT}, 4× Interpolation

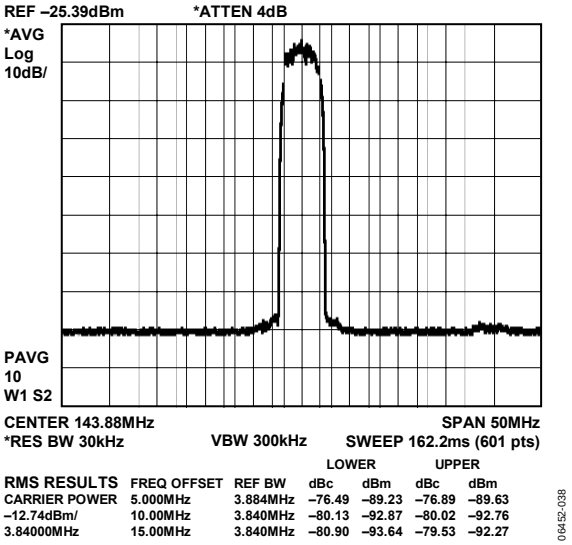


Figure 41. AD9778A ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

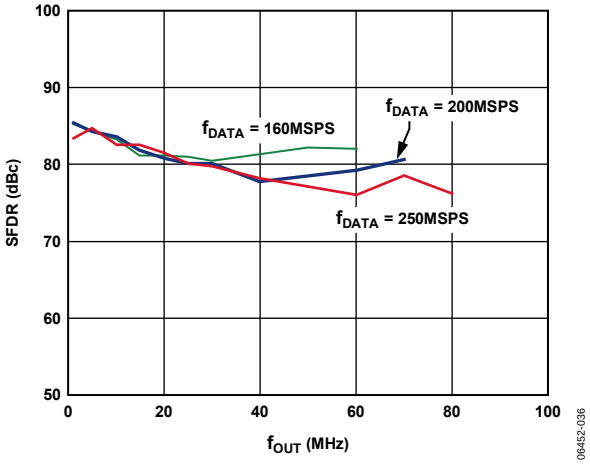


Figure 39. AD9778A In-Band SFDR vs. f_{OUT}, 2× Interpolation

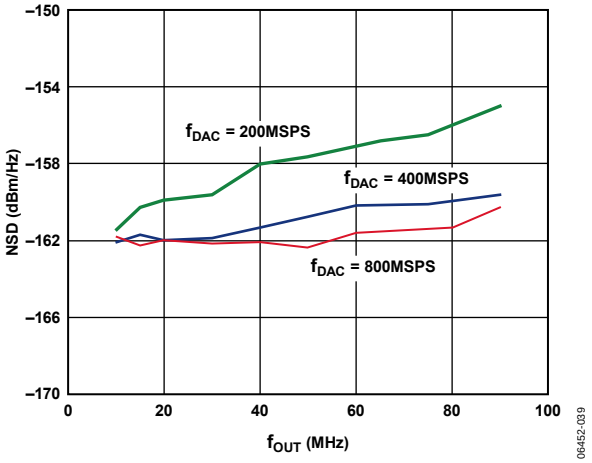


Figure 42. AD9778A Noise Spectral Density vs. f_{OUT} for Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

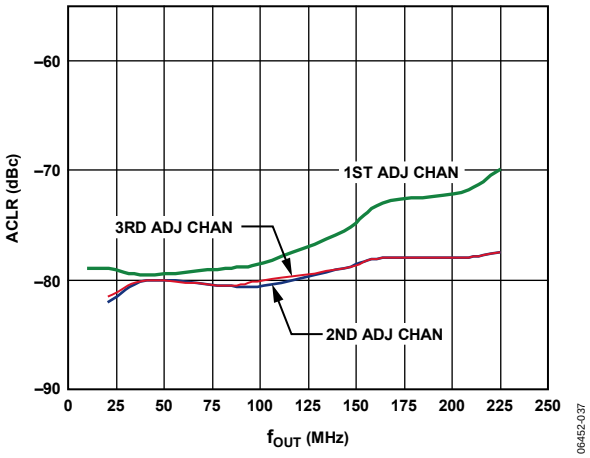


Figure 40. AD9778A ACLR, Single-Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

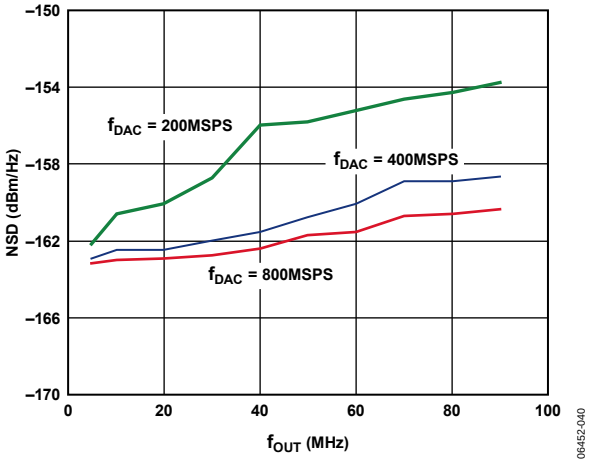


Figure 43. AD9778A Noise Spectral Density vs. f_{OUT} with Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

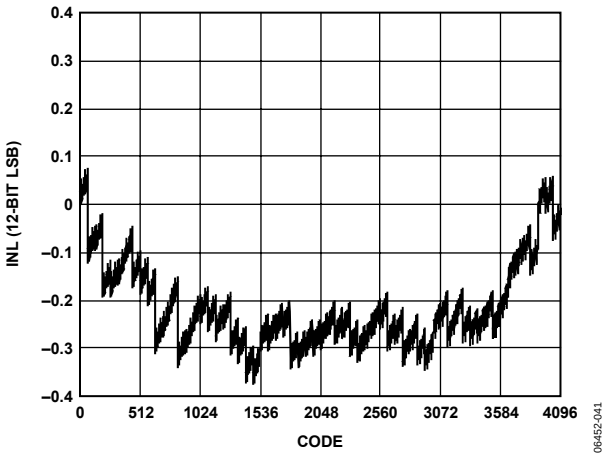


Figure 44. AD9776A Typical INL

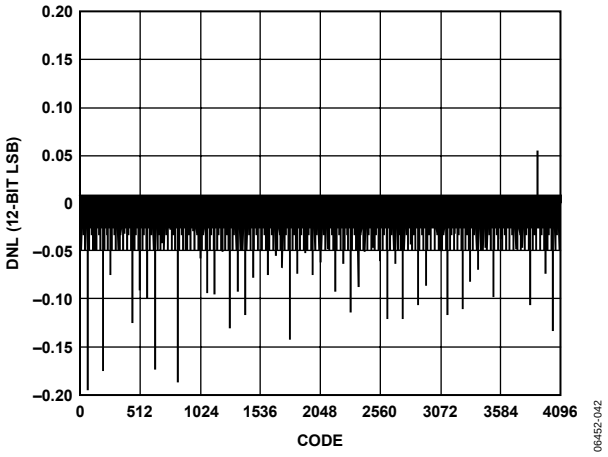


Figure 45. AD9776A Typical DNL

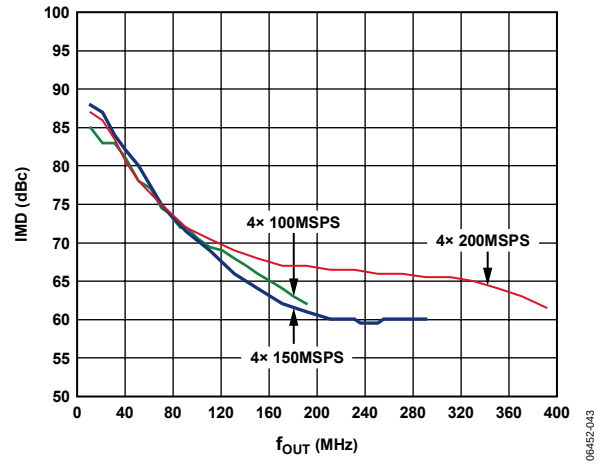


Figure 46. AD9776A IMD vs. f_{OUT}, 4× Interpolation

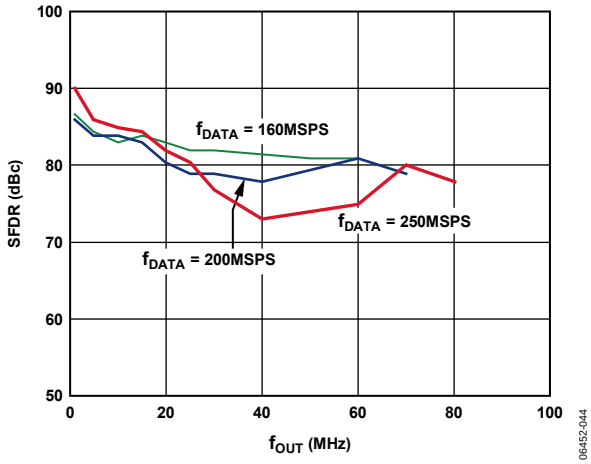


Figure 47. AD9776A In-Band SFDR vs. f_{OUT}, 2× Interpolation

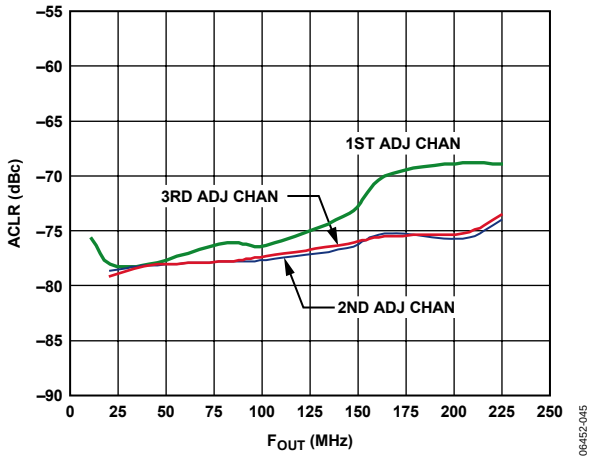


Figure 48. AD9776A ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, $f_{DAC}/4$ Modulation

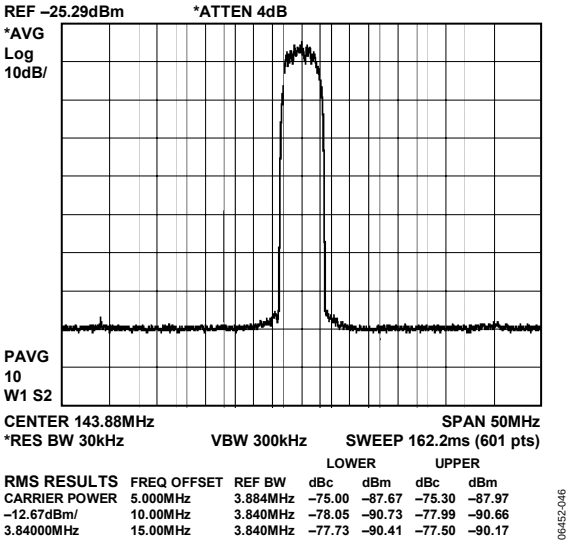


Figure 49. AD9776A, Single Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

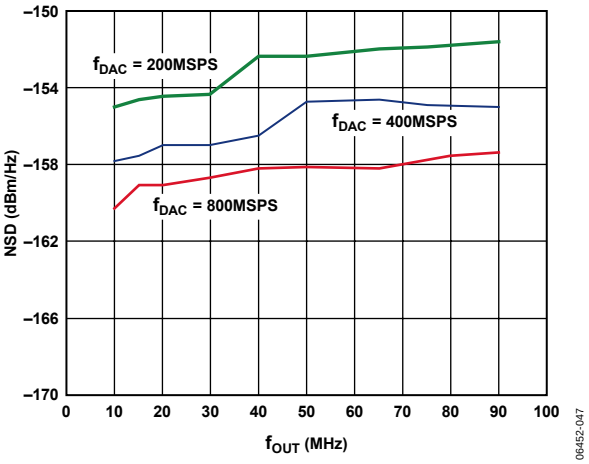


Figure 50. AD9776A Noise Spectral Density vs. f_{OUT}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

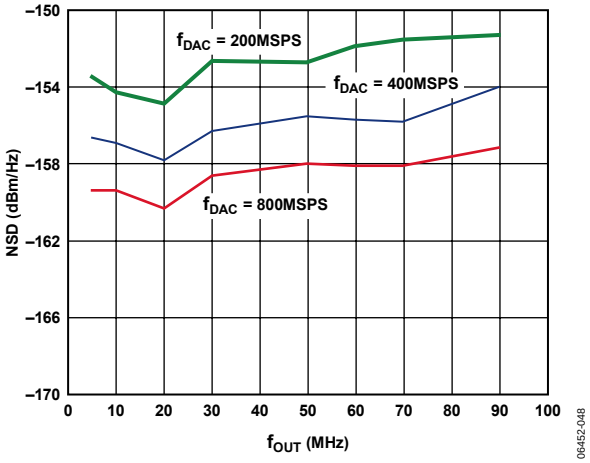


Figure 51. AD9776A Noise Spectral Density vs. f_{OUT}, Single-Tone Input at −6 dBFS, f_{DATA} = 200 MSPS

TERMINOLOGY

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current at Code 0 from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the difference between the full-scale output and bottom-scale output.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

In-Band Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Out-of-Band Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
The ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9776A/AD9778A/AD9779A combine many features to make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses an innovative filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to perform digital quadrature frequency upconversions. They also have features that allow simplified synchronization with incoming data and between multiple parts.

DIFFERENCES BETWEEN AD9776/AD9778/AD9779 AND AD9776A/AD9778A/AD9779A

REFCLK Max Frequency vs. Supply

A maximum sample rate of 1100 MHz is supported by certain restrictions on the DVDD18 and CVDD18 power supplies. Table 1 lists the valid operating frequencies vs. power supply voltage.

REFCLK Amplitude

With a differential sinusoidal clock applied to REFCLK, the PLL on the AD9776/AD9778/AD9779 does not achieve optimal noise performance unless the REFCLK differential amplitude is increased to 2 V p-p. Note that if an LVPECL driver is used on the AD9776/AD9778/AD9779, the PLL gives optimal performance if the REFCLK amplitude is well within LVPECL specifications (<1.6 V p-p diff). The design of the PLL on the AD9779A has been improved, so that even with a sinusoidal clock, the PLL still achieve optimal amplitude with the swing = 1.6 V p-p.

PLL Lock Ranges

See Table 19 and Figure 75 for PLL lock ranges for the AD9776A/AD9778A/AD9779A. The individual lock ranges for the AD9776A/AD9778A/AD9779A PLL are wider than those for the AD9776/AD9778/AD9779. This means that the AD9776A/AD9778A/AD9779A PLL remain in lock in a given range over a wider temperature range than the AD9776/AD9778/AD9779.

PLL Optimal Settings

See Table 17, the PLL Loop Filter Bandwidth section, and the AD9776A/AD9778A/AD9779A PLL Autosearch Feature section for the optimal PLL settings for these parts. Table 9 shows the optimal PLL settings for the AD9776/AD9778/AD9779 and AD9779A:

Input Data Delay Line, Manual and Automatic Correction Modes

The AD9776A/AD9778A/AD9779A can be programmed to sense when the timing margin on the input data falls below a preset threshold and to take action. The device can be programmed to either set the IRQ (pin and register) or automatically reoptimize the timing input data timing.

Input Data Timing

See Table 20 for timing specifications vs. temperature. The input data timing specifications (setup and hold) have changed in the AD9776A/AD9778A/AD9779A. They are not the same as the timing specifications in the AD9776/AD9778/AD9779.

Data Clock Delay Range has been Doubled

In the AD9776/AD9778/AD9779, the input data delay was controlled by Register 4, Bits<7:4>. At 25°C, the delay was stepped by approximately 180 ps/increment. In the AD9779A, an extra bit has been added which effectively doubles the delay range. This bit is now located at Register 1, Bit 1. The increment/step on the AD9776A/AD9778A/AD9779A remains at ~180 ps.

Version Register

The version register (Register 0x1F) of the AD9776A/AD9778A/AD9779A read a value of 0x03. The version register of the AD9776/AD9778/AD9779 read a value of 0x02.

Table 9.

Part No.	BW Adjustment Register 0x0A<4:0>	PLL Bias Setting Register 0x09<2:0>	Optimal PLL Readback Value Register 0x0A <7:5>
AD9779	11111	111	010
AD9776A/AD9778A/AD9779A	01111	011	011

SERIAL PERIPHERAL INTERFACE

The SPI port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The port is compatible with most synchronous transfer formats including both the Motorola SPI and Intel® SSR protocols.

The interface allows read and write access to all registers that configure the AD9776A/AD9778A/AD9779A. Single or multiple byte transfers are supported as well as MSB-first or LSB-first transfer formats. Serial data input/output can be accomplished through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

The serial port configuration is controlled by Register 0x00, Bits<7:6>. It is important to note that any change made to the serial port configuration occurs immediately upon writing to the last bit of this byte. Therefore, it is possible with a multibyte transfer to write to this register and change the configuration in the middle of a communication cycle. Care must be taken to compensate for the new configuration within the remaining bytes of the current communication cycle.

Use of a single-byte transfer when changing the serial port configuration is recommended to prevent unexpected device behavior.

As described in this section, all serial port data is transferred to/from the device in synchronization to the SCLK pin. If synchronization is lost, the device has the ability to asynchronously terminate an I/O operation, putting the serial port controller into a known state and, thereby, regaining synchronization.

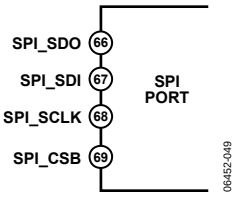


Figure 52. SPI Port

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9776A/AD9778A/AD9779A. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coinciding with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A Logic high on the CSB pin followed by a Logic low resets the SPI port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the other signal levels at the inputs to the SPI port. If the SPI port is in an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes as determined by the instruction byte. Using one multibyte transfer is preferred. Single-byte data transfers are useful in reducing CPU overhead when register access requires only one byte. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

See Table 10 for information contained in the instruction byte.

Table 10. SPI Instruction Byte

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

N1 and N0, Bit 6 and Bit 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The translation for the number of bytes to be transferred is listed in Table 11.

A4, A3, A2, A1, and A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0, respectively—of the instruction byte determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the device based on the LSB-first bit (Register 0x00, Bit 6).

Table 11. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer three bytes
1	0	Transfer two bytes
1	1	Transfer four bytes

Serial Interface Port Pin Descriptions

Serial Clock (SCLK)
The serial clock pin synchronizes data to and from the device as well as running the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select (CSB)
Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

Serial Data I/O (SDIO)
Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Out (SDO)
Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register Bit LSB/MSB First (Register 0x00, Bit 6). The default is MSB-first (LSB/MSB First = 0).

When LSB/MSB first = 0 (MSB-first) the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB First mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB/MSB-First = 1 (LSB first) the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB-first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB-first mode is active.

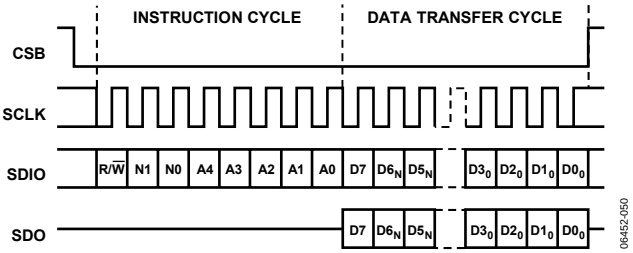


Figure 53. Serial Register Interface Timing MSB-First

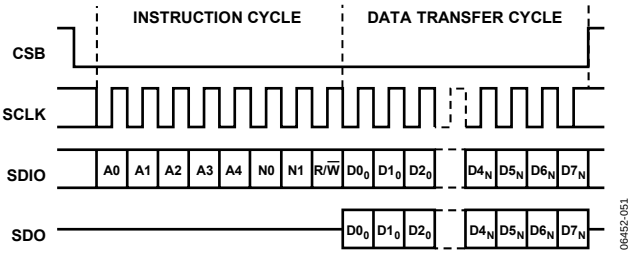


Figure 54. Serial Register Interface Timing LSB-First

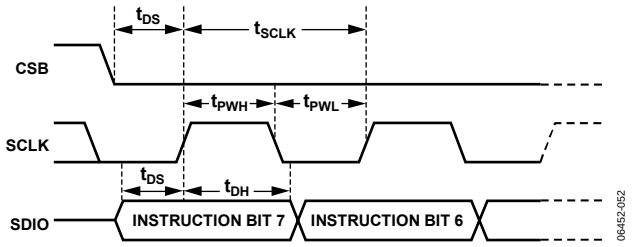


Figure 55. Timing Diagram for SPI Register Write

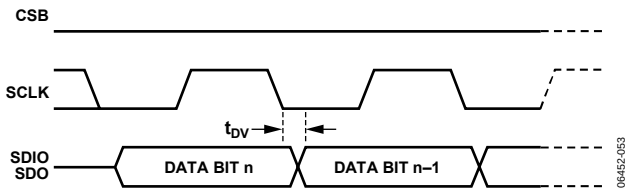


Figure 56. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Table 12.

Register Name	Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Comm	0x00	00	SDIO Bidirectional	LSB/MSB First	Software Reset	Power-Down Mode	Auto Power-Down Enable		PLL Lock Indicator (Read Only)		0x00
Digital Control	0x01	01	Filter Interpolation Factor<1:0>		Filter Modulation Mode<3:0>				Data Clock Delay MSB<4>	Zero Stuffing Enable	0x00
	0x02	02	Data Format	Dual/Interleaved Data Bus Mode	Real Mode	Data Clock Delay Enable	Inverse Sinc Enable	DATACLK Invert	TxEnable Invert	Q First	0x00
Sync Control	0x03	03	Data Clock Delay Mode	Reserved, Should Always Be Set High	Data Clock Divide Ratio<1:0>		Data Delay Timing Margin<3:0>				0x00
	0x04	04	Data Clock Delay LSBs<3:0>				Output Sync Pulse Divide<2:0>			Sync Out Delay<4>	0x00
	0x05	05	Sync Out Delay<3:0>				Input Sync Pulse Frequency Ratio<2:0>			Sync Input Delay<4>	0x00
	0x06	06	Sync Input Delay<3:0>				Input Sync Pulse Timing Error Tolerance<3:0>				0x00
	0x07	07	Sync Receiver Enable	Sync Driver Enable	Sync Triggering Edge	DAC Clock Offset<4:0>					0x00
PLL Control	0x08	08	PLL Band Select<5:0>						PLL VCO AGC Gain<1:0>		0xE7
	0x09	09	PLL Enable	PLL VCO Divider Ratio<1:0>		PLL Loop Divide Ratio<1:0>	PLL Bias Setting<2:0>				0x52
Misc Control	0x0A	10	PLL Control Voltage Range<2:0> (Read-Only)			PLL Loop Bandwidth Adjustment<4:0>					0x1F
I DAC Control Register	0x0B	11	I DAC Gain Adjustment<7:0>								0xF9
	0x0C	12	I DAC Sleep	I DAC Power Down					I DAC Gain Adjustment<9:8>		0x01
AUX DAC1 Control Register	0x0D	13	Auxiliary DAC1 Data <7:0>								0x00
	0x0E	14	Auxiliary DAC1 Sign	Auxiliary DAC1 Current Direction	Auxiliary DAC1 Power-Down				Auxiliary DAC1 Data<9:8>		0x00
Q DAC Control Register	0x0F	15	Q DAC Gain Adjustment<7:0>								0xF9
	0x10	16	Q DAC Sleep	Q DAC Power-Down					Q DAC Gain Adjustment<9:8>		0x01
AUX DAC2 Control Register	0x11	17	Auxiliary DAC2 Data<7:0>								0x00
	0x12	18	Auxiliary DAC2 Sign	Auxiliary DAC2 Current Direction	Auxiliary DAC2 Power-Down				Auxiliary DAC2 Data<9:8>		0x00
	0x13 to 0x18	19 to 24	Reserved								
Interrupt Register	0x19	25	Data Delay IRQ	Sync Delay IRQ		Setup Status IRQ	Data Delay IRQ Enable	Sync Delay IRQ Enable		Internal Sync Loopback	0x00
Version Register	0x1F	31	Version<7:0>								0x03

Table 13. SPI Register Description

Register Name	Address		Description	Function	Default
	Hex	Decimal			
Comm Register	00	7	SDIO bidirectional	0: use SDIO pin as input data only	0
				1: use SDIO as both input and output data	
	00	6	LSB/MSB first	0: first bit of serial data is MSB of data byte	0
				1: first bit of serial data is LSB of data byte	
	00	5	Software reset	Bit must be written with a 1, then 0 to soft reset SPI register map	0
	00	4	Power-down mode	0: all circuitry is active	
				1: disable all digital and analog circuitry, only SPI port is active	
	00	3	Auto power-down enable	Controls auto power-down mode, see the Power-Down and Sleep Modes section	0
	00	1	PLL lock indicator (read only)	0: PLL is not locked	
				1: PLL is locked	0
Digital Control Register	01	7:6	Filter interpolation factor<1:0>	00: 1× interpolation	00
				01: 2× interpolation	
				10: 4× interpolation	
				11: 8× interpolation	
	01	5:2	Filter modulation mode	See Table 18 for filter modes	0000
	01	1	Data Clock Delay MSB<4>	Sets delay of REFCLK in to DATACLK out	0
	01	0	Zero stuffing enable	0: zero stuffing off	0
				1: zero stuffing on	
	02	7	Data format	0: signed binary	0
				1: unsigned binary	
	02	6	Dual/interleaved data bus mode	0: both input data ports receive data	0
				1: Data Port 1 only receives data	
	02	5	Real mode	0: enable Q path for signal processing	0
				1: disable Q path data (internal Q channel clocks disabled, I and Q modulators disabled)	
	02	4	data clock delay enable	Enables the DATACLK delay feature. More details on this feature are shown in the Using Data Delay to Meet Timing Requirements section	
	02	3	Inverse sinc enable	0: inverse sinc filter disabled	0
				1: inverse sinc filter enabled	
	02	2	DATACLK invert	0: output DATACLK same phase as internal capture clock	0
				1: output DATACLK opposite phase as internal capture clock	
	02	1	TxEnable invert	Inverts the function of TxEnable Pin 39, see the Interleaved Data Mode section	0
	02	0	Q first	0: first byte of data is always I data at the beginning of transmit	
				1: first byte of data is always Q data at the beginning of transmit	
Sync Control Register	03	7	Data clock delay mode	0: manual error detect mode	0
				1: auto error correct mode	
	03	6	Reserved	Should always be set to 1	0
	03	5:4	Data clock divide ratio<1:0>	DATACLK output divider value	00
				00: divide by 1	
				01: divide by 2	
				10: divide by 4	
				11: divide by 1	

Register Name	Address		Description	Function	Default
	Hex	Decimal			
	03	3:0	Data delay timing margin<3:0>	See Table 21	0000
	04	7:4	Data clock delay LSBs<3:0>	Sets delay of REFCLK in to DATACLK out	0000
	04	3:1	Output SYNC pulse divide<2:0>	The frequency of the SYNC_O signal is equal to f_{DAC}/N, where N is set as follows: 000: N = 32 001: N = 16 010: N = 8 011: N = 4 100: N = 2 101: N = 1 110: N = undefined 111: N = undefined	000
	04	0	Sync out delay<4>	Sync output delay, Bit 4	
	05	7:4	Sync out delay<3:0>	Sync output delay, Bits<3:0> The delay line resolution is 180 ps per step	0000
	05	3:1	Input sync pulse frequency ratio<2:0>	Input sync pulse frequency divider, see the AN-822 application note	000
	05	0	Sync input delay<4>	Sync input delay, Bit 4	0
	06	7:4	Sync input delay<3:0>	See the Multiple DAC Synchronization section for details on using these registers to synchronize multiple DACs	0
	06	3:0	Input sync pulse timing error tolerance<3:0>		0
	07	7	SYNC receiver enable		0
	07	6	Sync driver enable		0
	07	5	Sync triggering edge	0: SYNC_O changes on REFCLK falling edge 1: SYNC_O changes on REFCLK rising edge	0
	07	4:0	Data clock offset<4:0>		0
PLL Control	08	7:2	PLL band select<5:0>	VCO frequency range vs. PLL band select value (see Table 19)	111001
	08	1:0	PLL VCO AGC gain<10>	Leave at default value for optimal performance	11
	09	7	PLL enable	0: PLL off, DAC rate clock supplied by outside source 1: PLL on, DAC rate clock synthesized internally from external reference clock via PLL clock multiplier	0
	09	6:5	PLL VCO divider ratio<1:0>	FVCO/f_{DAC} 00 × 1 01 × 2 10 × 4 11 × 8	10
	09	4:3	PLL loop divide ratio<1:0>	f_{DAC}/f_{REF} 00 × 2 01 × 4 10 × 8 11 × 16	10
	09	2:0	PLL bias setting<2:0>	Set to 011 for optimal performance	010
Misc Control	0A	7:5	PLL control voltage range<2:0>	000 to 111, proportional to voltage at PLL loop filter output, readback only	000
	0A	4:0	PLL loop bandwidth adjustment<4:0>	See PLL Loop Filter Bandwidth section for details, optimally set at 0x0F	11111

Register Name	Address Hex	Address Decimal	Description	Function	Default
I DAC Control Register	0B	7:0	I DAC gain adjustment<7:0>	LSB I DAC 10-bit gain setting word	11111001
	0C	7	I DAC sleep	0: I DAC on 1: I DAC off	0
	0C	6	I DAC power-down	0: I DAC on 1: I DAC off	0
	0C	1:0	I DAC gain adjustment	MSB I DAC 10-bit gain setting word	01
AUX DAC1 Control Register	0D	7:0	Auxiliary DAC1 data<7:0>	LSB AUX DAC1 10-bit gain setting word	00000000
	0E	7	Auxiliary DAC1 sign	0: AUX1_P active 1: AUX1_N active	
	0E	6	Auxiliary DAC1 current direction	0: source 1: sink	0
	0E	5	Auxiliary DAC1 power-down	0: AUX DAC1 on 1: AUX DAC1 off	0
	0E	1:0	Auxiliary DAC1 data<9:8>	MSB AUX DAC1 10-bit gain setting word	00
Q DAC Control Register	0F	7:0	Q DAC gain adjustment<7:0>	LSB Q DAC 10-bit gain setting word	11111001
	10	7	Q DAC sleep	0: Q DAC on 1: Q DAC off	0
	10	6	Q DAC power-down	0: Q DAC on 1: Q DAC off	0
	10	1:0	Q DAC gain adjustment<9:8>	MSB Q DAC 10-bit gain setting word	
AUX DAC2 Control Register	11	7:0	Auxiliary DAC2 data<7:0>	LSB AUX DAC2 10-bit gain setting word	00000000
	12	7	Auxiliary DAC2 Sign	0: AUX2_P active 1: AUX2_N active	
	12	6	Auxiliary DAC2 current direction	0: source 1: sink	0
	12	5	Auxiliary DAC2 power-down	0: AUX DAC2 on 1: AUX DAC2 off	0
	12	1:0	Auxiliary DAC2 data<9:8>	MSB AUX DAC2 10-bit gain setting word	00
Interrupt Register	19	7	Data delay IRQ	Readback, must write 0 to clear	0
	19	6	Sync delay IRQ	Readback, must write 0 to clear	0
	19	5			0
	19	4	Setup status IRQ	When DATA DELAY IRQ is set, this bit represents the following: 0: hold error 1: set up error Enabled when DATA DELAY IRQ is enabled	
	19	3	Data delay IRQ enable		0
	19	2	Sync delay IRQ enable		0
	19	0	Internal sync loopback		0
Version Register	1F	7:0	Version<7:0>	Indicates device hardware revision number	

INTERPOLATION FILTER ARCHITECTURE

The AD9776A/AD9778A/AD9779A can provide up to 8× interpolation, or the interpolation filters can be entirely disabled. It is important to note that the input signal should be backed off by approximately 0.01 dB from full scale to avoid overflowing the interpolation filters. The coefficients of the low-pass filters and the inverse sinc filter are given in Table 14, Table 15, Table 16, and Table 17. Spectral plots for the filter responses are shown in Figure 57, Figure 58, and Figure 59.

Table 14. Half-Band Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	−4
H(2)	H(54)	0
H(3)	H(53)	+13
H(4)	H(52)	0
H(5)	H(51)	−34
H(6)	H(50)	0
H(7)	H(49)	+72
H(8)	H(48)	0
H(9)	H(47)	−138
H(10)	H(46)	0
H(11)	H(45)	+245
H(12)	H(44)	0
H(13)	H(43)	−408
H(14)	H(42)	0
H(15)	H(41)	+650
H(16)	H(40)	0
H(17)	H(39)	−1003
H(18)	H(38)	0
H(19)	H(37)	+1521
H(20)	H(36)	0
H(21)	H(35)	−2315
H(22)	H(34)	0
H(23)	H(33)	+3671
H(24)	H(32)	0
H(25)	H(31)	−6642
H(26)	H(30)	0
H(27)	H(29)	+20,755
H(28)		+32,768

Table 15. Half-Band Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	−2
H(2)	H(22)	0
H(3)	H(21)	+17
H(4)	H(20)	0
H(5)	H(19)	−75
H(6)	H(18)	0
H(7)	H(17)	+238
H(8)	H(16)	0
H(9)	H(15)	−660
H(10)	H(14)	0
H(11)	H(13)	+2530
H(12)		+4096

Table 16. Half-Band Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	−39
H(2)	H(14)	0
H(3)	H(13)	+273
H(4)	H(12)	0
H(5)	H(11)	−1102
H(6)	H(10)	0
H(7)	H(9)	+4964
H(8)		+8192

Table 17. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	+2
H(2)	H(8)	−4
H(3)	H(7)	+10
H(4)	H(6)	−35
H(5)		+401

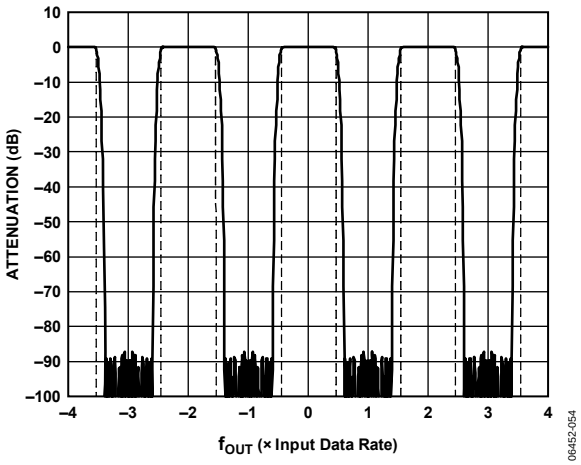


Figure 57. 2× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

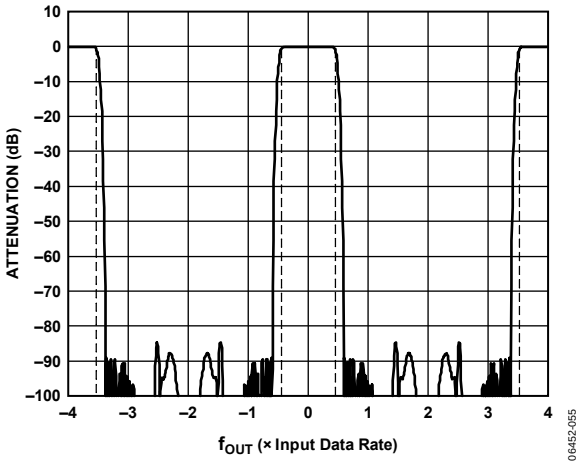


Figure 58. 4× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

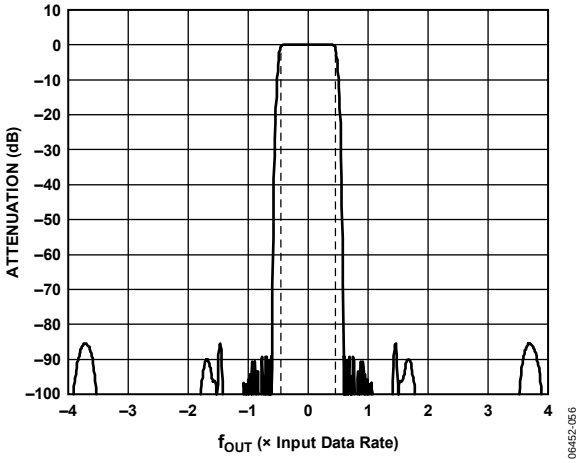


Figure 59. 8× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

With the interpolation filter and modulator combined, the incoming signal can be placed anywhere within the Nyquist region of the DAC output sample rate. When the input signal is complex, this architecture allows modulation of the input signal to positive or negative Nyquist regions (see Table 18).

The Nyquist regions of up to 4× the input data rate can be seen in Figure 60.

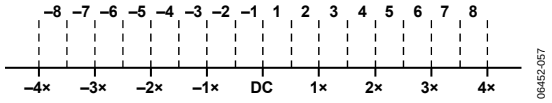


Figure 60. Nyquist Zones

Figure 57, Figure 58, and Figure 59 show the low-pass response of the digital filters with no modulation. By turning on the modulation feature, the response of the digital filters can be tuned to anywhere within the DAC bandwidth. As an example, Figure 61 to Figure 67 show the nonshifted mode filter responses (refer to Table 18 for shifted/nonshifted mode filter responses).

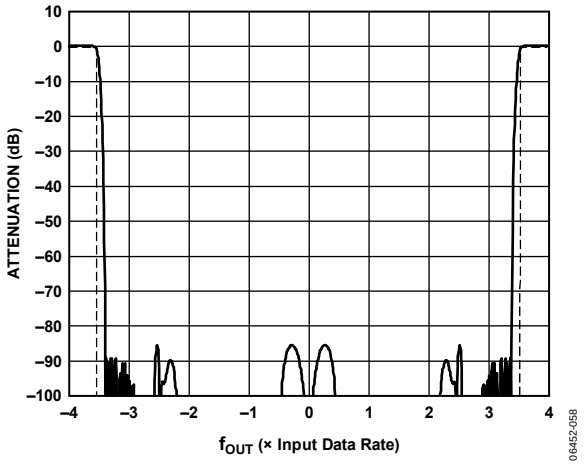


Figure 61. Interpolation/Modulation Combination of $4f_{DAC}/8$ Filter

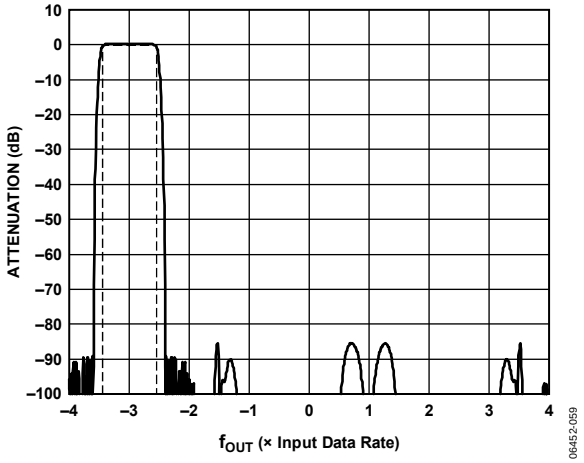


Figure 62. Interpolation/Modulation Combination of $-3f_{DAC}/8$ Filter

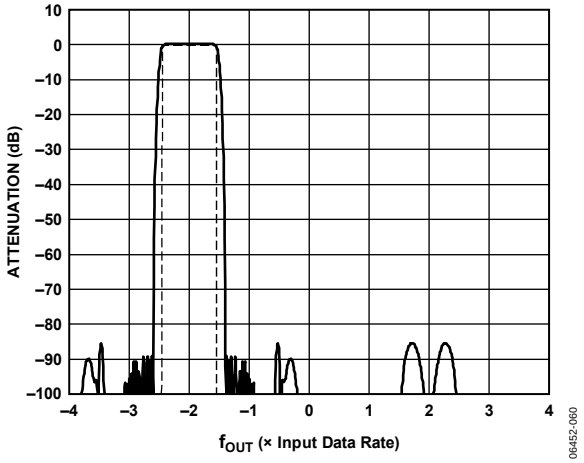


Figure 63. Interpolation/Modulation Combination of $-2f_{DAC}/8$ Filter

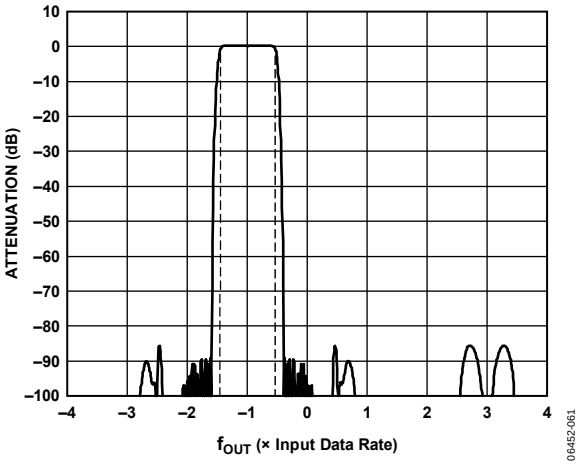


Figure 64. Interpolation/Modulation Combination of –1f_{DAC}/8 Filter

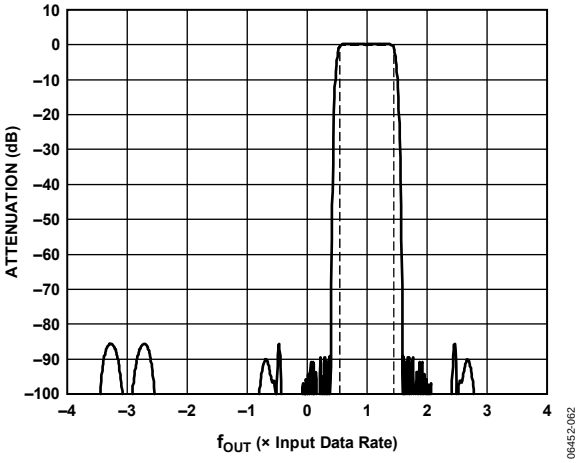


Figure 65. Interpolation/Modulation Combination of f_{DAC}/8 Filter

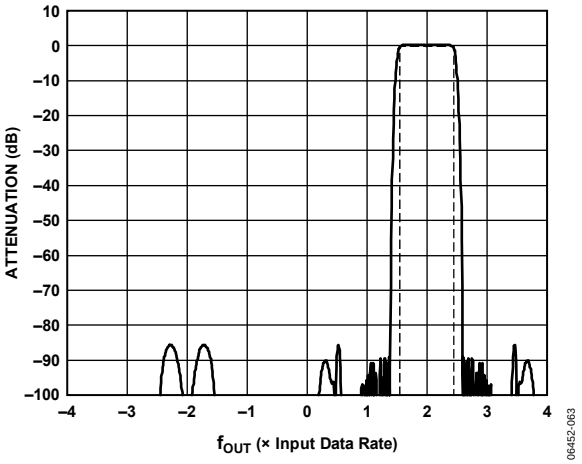


Figure 66. Interpolation/Modulation Combination of 2f_{DAC}/8 Filter

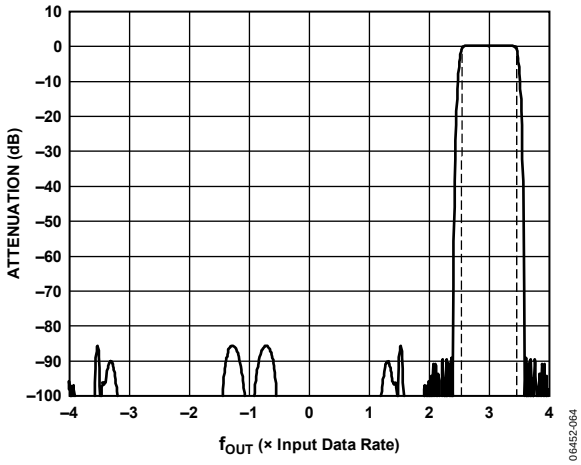


Figure 67. Interpolation/Modulation Combination of 3f_{DAC}/8 Filter

Shifted mode filter responses allow the pass band to be centered around ±0.5 f_{DATA}, ±1.5 f_{DATA}, ±2.5 f_{DATA}, and ±3.5 f_{DATA}. Switching to the shifted mode response does not modulate the signal. Instead, the pass band is simply shifted. For example, picture the response shown in Figure 67 and assume the signal in-band is a complex signal over the bandwidth 3.2 f_{DATA} to 3.3 f_{DATA}. If the shifted mode filter response is then selected, the pass band becomes centered at 3.5 f_{DATA}. However, the signal remains at the same place in the spectrum. The shifted mode capability allows the filter pass band to be placed anywhere in the DAC Nyquist bandwidth.

The AD9776A/AD9778A/ AD9779A are dual DACs with internal complex modulators built into the interpolating filter response. In dual channel mode, the devices expect the real and the imaginary components of a complex signal at Digital Input Port 1 and Digital Input Port 2 (I and Q, respectively). The DAC outputs then represent the real and imaginary components of the input signal, modulated by the complex carrier (f_{DAC}/2, f_{DAC}/4, or f_{DAC}/8).

With Register 2, Bit 6 set, the device accepts interleaved data on Port 1 in the I, Q, I, Q . . . sequence. Note that in interleaved mode, the channel data rate at the beginning of the I and the Q data paths is now half the input data rate because of the interleaving. The maximum input data rate is still subject to the maximum specification of the device. This limits the synthesis bandwidth available at the input in interleaved mode.

With Register 0x02, Bit 5 (real mode) set, the Q channel and the internal I and Q digital modulation are turned off. The output spectrum at the I DAC then represents the signal at Digital Input Port 1, interpolated by 1×, 2×, 4×, or 8×.

The general recommendation is that if the desired signal is within ±0.4 × f_{DATA}, use the nonshifted filter mode. Outside of this, the shifted filter mode should be used. In any situation, the total bandwidth of the signal should be less than 0.8 × f_{DATA}.

Table 18. Interpolation Filter Modes, (Register 0x01, Bits<5:2>)

Interpolation Factor<7:6>	Filter Mode<5:2>	Modulation	Nyquist Zone Pass Band	F_Low[1]	Center[1]	F_High[1]	Comments
8	0x00	DC	+1	−0.05	0	+0.05	In 8× interpolation; BW (min) = 0.0375 × f_{DAC} BW (max) = 0.1 × f_{DAC}
8	0x01	DC shifted	+2	+0.0125	+0.0625	+0.1125	
8	0x02	F/8	+3	+0.075	+0.125	+0.175	
8	0x03	F/8 shifted	+4	+0.1375	+0.1875	+0.2375	
8	0x04	F/4	+5	+0.2	+0.25	+0.3	
8	0x05	F/4 shifted	+6	+0.2625	+0.3125	+0.3625	
8	0x06	3F/8	+7	+0.325	+0.375	+0.425	
8	0x07	3F/8 shifted	+8	+0.3875	+0.4375	+0.4875	
8	0x08	F/2	−8	−0.55	−0.5	−0.45	
8	0x09	F/2 shifted	−7	−0.4875	−0.4375	−0.3875	
8	0x0A	−3F/8	−6	−0.425	−0.375	−0.343	
8	0x0B	−3F/8 shifted	−5	−0.3625	−0.3125	−0.2625	
8	0x0C	−F/4	−4	−0.3	−0.25	−0.2	
8	0x0D	−F/4 shifted	−3	−0.2375	−0.1875	−0.1375	
8	0x0E	−F/8	−2	−0.175	−0.125	−0.075	
8	0x0F	−F/8 shifted	−1	−0.1125	−0.0625	−0.0125	
4	0x00	DC	+1	−0.1	0	+0.1	In 4× interpolation; BW (min) = 0.075 × f_{DAC} BW (max) = 0.2 × f_{DAC}
4	0x01	DC shifted	+2	+0.025	+0.125	+0.225	
4	0x02	F/4	+3	+0.15	+0.25	+0.35	
4	0x03	F/4 shifted	+4	+0.275	0.375	0.475	
4	0x04	F/2	−4	−0.6	−0.5	−0.4	
4	0x05	F/2 shifted	−3	−0.475	−0.375	−0.275	
4	0x06	−F/4	−2	−0.35	−0.25	−0.15	
4	0x07	−F/4 shifted	−1	−0.225	−0.125	−0.025	
2	0x00	DC	+1	−0.2	0	+0.2	In 2× interpolation; BW (min) = 0.15 × f_{DAC} BW (max) = 0.4 × f_{DAC}
2	0x01	DC shifted	+2	+0.05	+0.25	+0.45	
2	0x02	F/2	−2	−0.7	−0.5	−0.3	
2	0x03	F/2 shifted	−1	−0.45	−0.25	−0.05	

[1] Frequency normalized to f_{DAC}.

INTERPOLATION FILTER MINIMUM AND MAXIMUM BANDWIDTH SPECIFICATIONS

The AD9776A/AD9778A/AD9779A use a novel interpolation filter architecture that allows DAC IF frequencies to be generated anywhere in the spectrum. Figure 68 shows the traditional choice of DAC IF output bandwidth placement. Note that there are no possible filter modes in which the carrier can be placed near 0.5 × f_{DATA}, 1.5 × f_{DATA}, 2.5 × f_{DATA}, and so on.

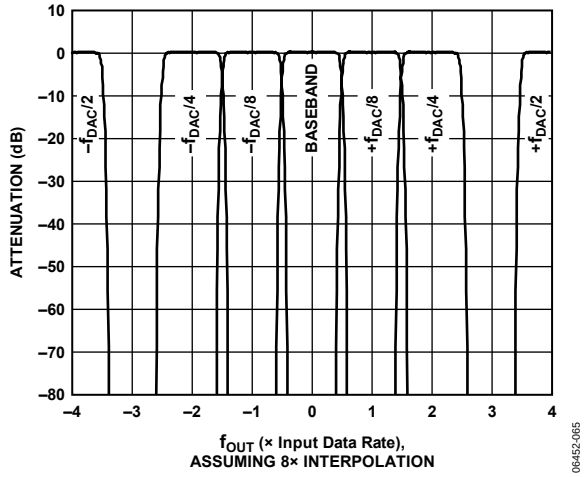


Figure 68. Traditional Bandwidth Options for TxDAC Output IF

The filter architecture not only allows the interpolation filter pass bands to be centered in the middle of the input Nyquist zones (as explained in this section), but also allows the possibility of a 3 × f_{DAC}/8 modulation mode. With all of these filter combinations, a carrier of given bandwidth can be placed anywhere in the spectrum and fall into a possible pass band of the interpolation filters. The possible bandwidths accessible with the filter architecture are shown in Figure 69 and Figure 70. Note that the shifted and nonshifted filter modes are all accessible by programming the filter mode for the particular interpolation rate.

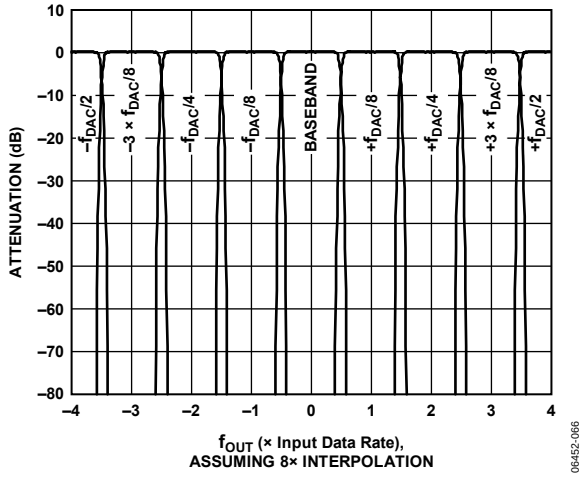


Figure 69. Nonshifted Bandwidths Accessible with the Filter Architecture

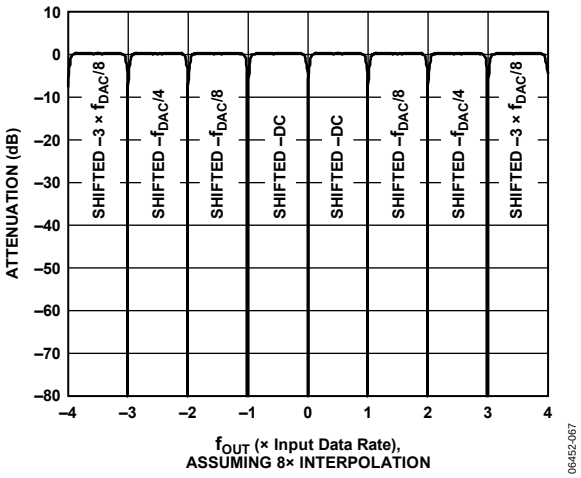


Figure 70. Shifted Bandwidths Accessible with the Filter Architecture

With this filter architecture, a signal placed anywhere in the spectrum is possible. However, the signal bandwidth is limited by the input sample rate of the DAC and the specific placement of the carrier in the spectrum. The bandwidth restriction resulting from the combination of filter response and input sample rate is often referred to as the synthesis bandwidth, because this is the largest bandwidth that the DAC can synthesize.

The maximum bandwidth condition exists if the carrier is placed directly in the center of one of the filter pass bands. In this case, the total 0.1 dB bandwidth of the interpolation filters is equal to 0.8 × f_{DATA}. As Table 18 shows, the synthesis bandwidth as a fraction of the DAC output sample rate drops by a factor of 2 for every doubling of interpolation rate. The minimum bandwidth condition exists, for example, if a carrier is placed at 0.25 × f_{DATA}. In this situation, if the nonshifted filter response is enabled, the high end of the filter response cuts off at 0.4 × f_{DATA}, thus limiting the high end of the signal bandwidth. If the shifted filter response is enabled instead, then the low end of the filter response cuts off at 0.1 × f_{DATA}, thus limiting the low end of the signal bandwidth. The minimum bandwidth specification that applies for a carrier at 0.25 × f_{DATA} is therefore 0.3 × f_{DATA}. The minimum bandwidth behavior is repeated over the spectrum for carriers placed at (±n ± 0.25) × f_{DATA}, where n is any integer.

DRIVING THE REFCLK INPUT

The REFCLK input requires a low jitter differential drive signal. It is a PMOS input differential pair powered from the 1.8 V supply, therefore, it is important to maintain the specified 400 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p about the 400 mV common-mode voltage. Although these input levels are not directly LVDS-compatible, REFCLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 71.

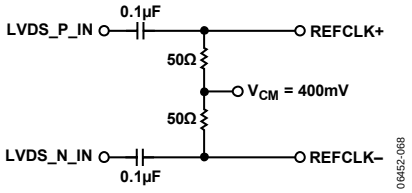


Figure 71. LVDS REFCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to REFCLK, as shown in Figure 71. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS to LVDS translator, then ac-coupled, as described in this section. Alternatively, it can be transformer-coupled and clamped, as shown in Figure 72.

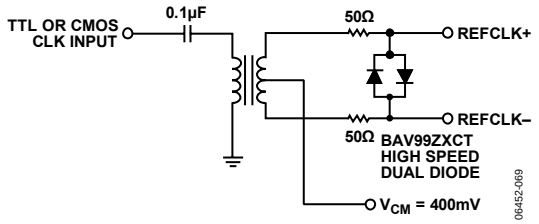


Figure 72. TTL or CMOS REFCLK Drive Circuit

A simple bias network for generating V_{CM} is shown in Figure 73. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade DAC performance.

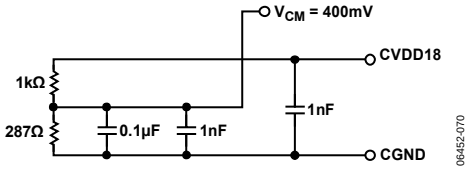


Figure 73. REFCLK V_{CM} Generator Circuit

INTERNAL PLL CLOCK MULTIPLIER/CLOCK DISTRIBUTION

The internal clock structure on the devices allows the user to drive the differential clock inputs with a clock at 1× or an integer multiple of the input data rate up to the DAC output sample rate. An internal PLL provides input clock multiplication and provides all the internal clocks required for the interpolation filters and data synchronization.

The internal clock architecture is shown in Figure 74. The reference clock is the differential clock at Pin 5 and Pin 6. This clock input can be run differentially or singled-ended by driving Pin 5 with a clock signal and biasing Pin 6 to the midswing point of the signal at Pin 5. The clock architecture can be run in the following configurations:

PLL Enabled (Register 0x09, Bit 7 = 1)

The PLL enable switch shown in Figure 74 is connected to the junction of the N_1 dividers (PLL VCO divide ratio) and N_2 dividers (PLL loop divide ratio). Divider N_3 determines the interpolation rate of the DAC, and the ratio N_3/N_2 determines the ratio of reference clock/input data rate. The VCO runs optimally over the range of 1.0 GHz to 2.0 GHz, so that N_1 keeps the speed of the VCO within this range, although the DAC sample rate can be lower. The loop filter components are entirely internal and no external compensation is necessary.

PLL Disabled (Register 0x09, Bit 7 = 0)

The PLL enable switch shown in Figure 74 is connected to the reference clock input. The differential reference clock input is the same as the DAC output sample rate. N_3 determines the interpolation rate.

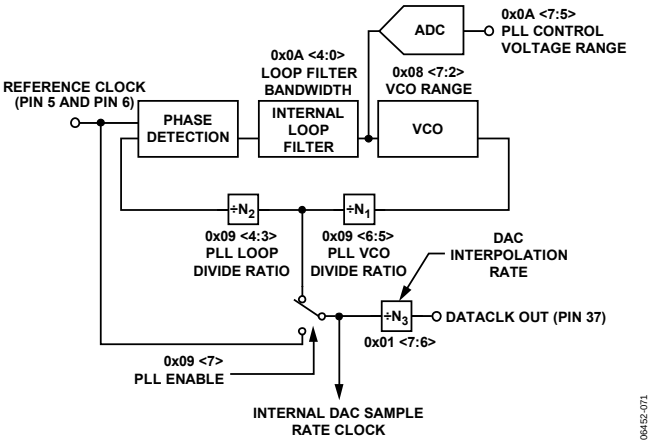


Figure 74. Internal Clock Architecture

Table 19. VCO Frequency Range vs. PLL Band Select Value

PLL Lock Ranges over Temp, −40°C to at +85°C		
	VCO Frequency Range in MHz	
PLL Band Select	f_{LOW}	f_{HIGH}
111111 (63)	Auto mode	
111110 (62)	1975	2026
111101 (61)	1956	2008
111100 (60)	1938	1992
111011 (59)	1923	1977
111010 (58)	1902	1961
111001 (57)	1883	1942
111000 (56)	1870	1931
110111 (55)	1848	1915
110110 (54)	1830	1897
110101 (53)	1822	1885
110100 (52)	1794	1869
110011 (51)	1779	1853
110010 (50)	1774	1840
110001 (49)	1748	1825
110000 (48)	1729	1810
101111 (47)	1730	1794
101110 (46)	1699	1780
101101 (45)	1685	1766
101100 (44)	1684	1748
101011 (43)	1651	1729
101010 (42)	1640	1702
101001 (41)	1604	1681
101000 (40)	1596	1658
100111 (39)	1564	1639
100110 (38)	1555	1606
100101 (37)	1521	1600
100100 (36)	1514	1575
100011 (35)	1480	1553
100010 (34)	1475	1529
100001 (33)	1439	1505
100000 (32)	1435	1489
011111 (31)	1402	1468
011110 (30)	1397	1451
011101 (29)	1361	1427
011100 (28)	1356	1412
011011 (27)	1324	1389
011010 (26)	1317	1375
011001 (25)	1287	1352
011000 (24)	1282	1336
010111 (23)	1250	1313
010110 (22)	1245	1299
010101 (21)	1215	1277
010100 (20)	1210	1264
010011 (19)	1182	1242
010010 (18)	1174	1231
010001 (17)	1149	1210
010000 (16)	1141	1198
001111 (15)	1115	1178
001110 (14)	1109	1166
001101 (13)	1086	1145
001100 (12)	1078	1135
001011 (11)	1055	1106
001010 (10)	1047	1103
001001 (9)	1026	1067
001000 (8)	1019	1072
000111 (7)	998	1049
000110 (6)	991	1041
000101 (5)	976	1026
000100 (4)	963	1011
000011 (3)	950	996
000010 (2)	935	981
000001 (1)	922	966
000000 (0)	911	951

VCO Frequency Ranges

Because the PLL band covers greater than a 2× frequency range, there can be two options for the PLL band select: one at the low end of the range and one at the high end of the range. Under these conditions, the VCO phase noise is optimal when the user selects the band select value corresponding to the high end of the frequency range. Figure 75 shows how the VCO bandwidth and the optimal VCO frequency varies with the band select value.

VCO Frequency Ranges over Temperature

The specifications given over temperature in Table 19 are for a single part in a single lot. Part-to-part and lot-to-lot these specifications can exhibit a mean shift of several register settings. Systems should be designed to take this potential shift into account to maintain optimal PLL performance.

In a system that may see wide temperature swings, it may be necessary for the user to sense the edges of the currently used lock range. The user would then switch to the next lock range to avoid potentially losing lock on the PLL.

PLL LOOP FILTER BANDWIDTH

The loop filter bandwidth of the PLL is programmed via SPI Register 0x0A, Bits<4:0>. Changing these values switches capacitors on the internal loop filter. No external loop filter components are required. This loop filter has a pole at 0 (P1), and then a zero (Z1) pole (P2) combination. Z1 and P2 occur within a decade of each other. The location of the zero pole is determined by Bits<4:0>. For a setting of 00000, the zero pole occurs near 10 MHz. By setting Bits<4:0> to 11111, the Z1/P2 combination can be lowered to approximately 1 MHz. The relationship between Bits<4:0> and the position of the Z1/P2 between 1 MHz and 10 MHz is linear. However, the internal components are not low tolerance and can drift by as much as ±30%.

For optimal performance, the bandwidth adjustment (Register 0x0A, Bits<4:0>) should be set to 01111 for all operating modes with PLL enabled. The PLL bias settings (Register 0x09, Bits<2:0>) should be set to 011. The PLL control voltage (Register 0x0A, Bits<7:5>) is read back and is proportional to the dc voltage at the internal loop filter output. With the PLL bias settings given in this section, the readback from the PLL control voltage should ideally be 011 or possibly 100 or 010. Anything outside of this range indicates that the PLL is not operating optimally.

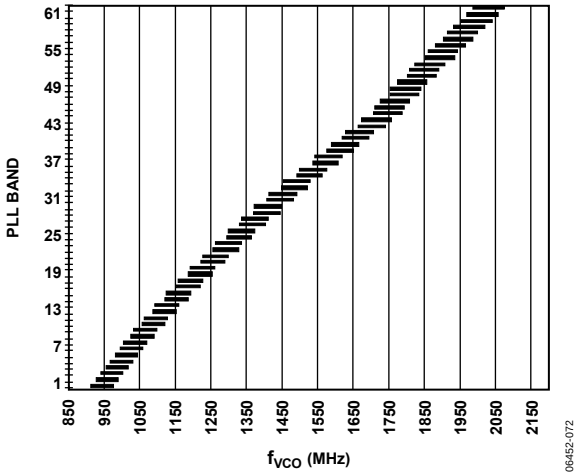


Figure 75. Typical PLL Band Select vs. Frequency over Temperature

AD9776A/AD9778A/AD9779A PLL AUTOSEARCH FEATURE

The AD9776A/AD9778A/AD9779A have an autosearch feature that determines the optimal band for the PLL. To enable the autosearch mode, set Register 0x08, Bits<7:2> to 11111b (63), and read back the value from Register 0x08, Bits<7:2>. Autosearch mode is intended to find the optimal PLL band only, after which the same settings should be applied in manual mode. It is not recommended that the PLL be set to autosearch mode during regular operation.

There are two ways in which the autosearch feature can be used. The first method is if the unit is in an environment where it is always started at ~25°C. In this case, the autosearch feature can be used to read back the optimal lock range value, and this value can then be immediately programmed into the lock range register. Started and programmed under this condition, the AD9776A/AD9778A/AD9779A are guaranteed to hold PLL lock over the entire operating temperature range. In this situation, autosearch only needs to be enabled when the unit is powered on. After the initial readback and programming the readback value into the lock range register, disable autosearch.

The second method for programming the PLL lock range in the AD9776A/AD9778A/AD9779A should be used if the unit is expected to start up under more extreme temperature shifts. For the AD9776A/AD9778A/AD9779A PLL to remain locked over the complete operating temperature range, the user should perform the following test in the factory at 25°C:

Enable the autosearch mode and read back the optimal value from the lock range register. Store this value in system memory (RAM, FPGA, ASIC).

As long as the unit is always programmed with this stored 25°C value on start-up, the PLL in the AD9776A/AD9778A/AD9779A is guaranteed to remain locked over the full temperature range of the part. This is true regardless of what the start-up temperature is of the unit.

Note that the autosearch mode only gives an accurate lock range, valid over the entire temperature range if the autosearch mode is enabled at 25°C. When the lock range at 25°C is determined and the value is stored, the autosearch mode should then be disabled. See AN-919 at www.analog.com for more information for valid lock ranges over temperature.

FULL-SCALE CURRENT GENERATION

Internal Reference

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to I120 (Pin 75). A simplified block diagram of the reference circuitry is shown in Figure 76. The recommended value for the external resistor is 10 kΩ, which sets up an $I_{REFERENCE}$ in the resistor of 120 μA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Internal current mirrors provide a current-gain scaling, where I DAC or Q DAC gain is a 10-bit word in the SPI port register (Register 0x0B, Register 0x0C, Register 0x0F, and Register 0x10). The default value for the DAC gain registers gives an I_{FS} of approximately 20 mA. I_{FS} is equal to

$$I_{FS} = \frac{1.2\text{ V}}{\text{R}} \times \left(\frac{27}{12} + \left(\frac{6}{1024} \times DAC\ gain \right) \right) \times 32$$

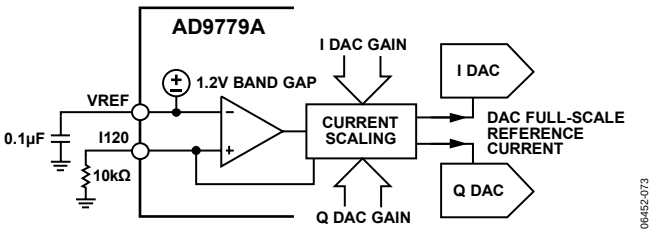


Figure 76. Reference Circuitry

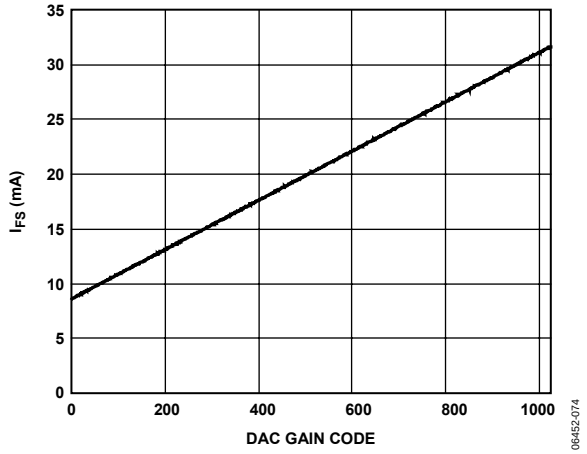


Figure 77. I_{FS} vs. DAC Gain Code

Application of Auxiliary DACs in Single Sideband Transmitter

Two auxiliary DACs are provided on the AD9776A/AD9778A/AD9779A. The full-scale output current on these DACs is derived from the 1.2 V band gap reference and external resistor between the I120 pin and ground. The gain scale from the reference amplifier current $I_{REFERENCE}$ to the auxiliary DAC reference current is 16.67 with the auxiliary DAC gain set to full scale (10-bit values, SPI Register 0x0D, and SPI Register 0x11), this gives a full-scale current of approximately 2 mA for auxiliary DAC1 and auxiliary DAC2.

The AUX DAC structure is shown in Figure 78. Only one of the two output pins of the AUX DAC is active at a time. The inactive side goes to a high impedance state (>100 kΩ). The active output pin is chosen by writing to Register 0x0E and Register 0x10, Bit 7.

The active output can act as either a current source or a current sink. When sourcing current, the output compliance voltage is 0 V to 1.6 V. When sinking current, the output compliance voltage is 0.8 V to 1.6 V. The output pin is chosen to be a current source or current sink by writing to Register 0x0E and Register 0x10, Bit 6.

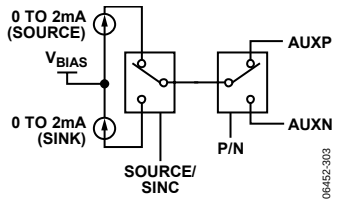


Figure 78. Auxiliary DAC Structure on AD9776A/AD9778A/AD97779A

The magnitude of the AUX DAC 1 current is controlled by the AUX DAC 1 Control Register 0x06, and the magnitude of the AUX DAC 2 current is controlled by the AUX DAC 2 Control Register 0x08. These AUX DACs have the ability to source or sink current. This is programmable via Bit 14 in either AUX DAC control register. The choice of sinking or sourcing should be made at circuit design time. There is no advantage to switching between source or sinking current once the circuit is in place.

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and can degrade system performance. Typical DAC-to-quadrature modulator interfaces are shown in Figure 79 and Figure 80. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling or a dc level shift is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, then the dc blocking capacitors in Figure 79 can be removed. A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect the system performance. Placing the filter at the location shown in Figure 79 and Figure 80 allows easy design of the filter, as the source and load impedances can easily be designed close to 50 Ω.

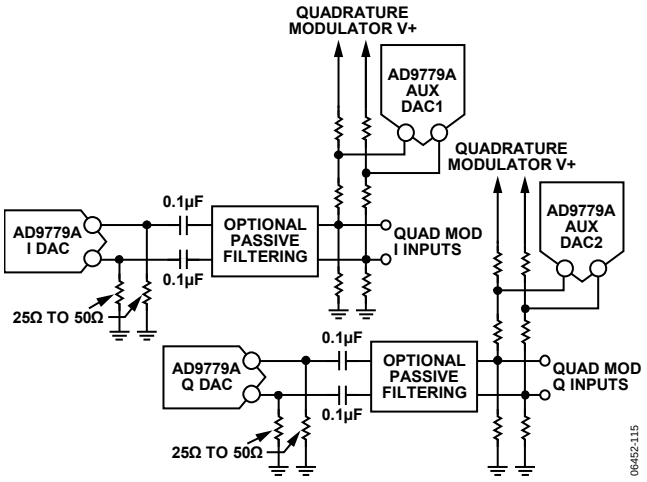


Figure 79. Typical Use of Auxiliary DACs AC Coupling to Quadrature Modulator

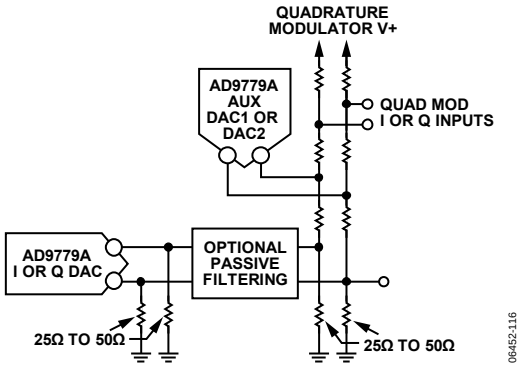


Figure 80. Typical Use of Auxiliary DACs DC Coupling to Quadrature Modulator with DC Shift

USING THE AD9776A/AD9778A/AD9779A TO CORRECT FOR NONIDEAL PERFORMANCE OF QUADRATURE MODULATORS ON THE IF TO RF CONVERSION

Analog quadrature modulators make it very easy to realize single sideband radios. However, there are several nonideal aspects of quadrature modulator performance. Among these analog degradations are

- Gain mismatch—The gain in the real and imaginary signal paths of the quadrature modulator may not be matched perfectly. This leads to less than optimal image rejection as the cancellation of the negative frequency image is less than perfect.
- LO feedthrough—The quadrature modulator has a finite dc referred offset, as well as coupling from its LO port to the signal inputs. These can lead to a significant spectral spurs at the frequency of the quadrature modulator LO.

The AD9776A/AD9778A/AD9779A has the capability to correct for both of these analog degradations. Understood that these degradations drift over temperature; therefore if close to optimal single sideband performance is desired, a scheme for sensing these degradations over temperature and correcting for them may necessary.

I/Q CHANNEL GAIN MATCHING

Gain matching is achieved by adjusting the values in the DAC gain registers. For the I DAC, these values are in the I DAC Control Register 0x05. For the Q DAC, these values are in the Q DAC Control Register 0x07. These are 10 bit values. To perform gain compensation, raise or lower the value of one of these registers by a fixed step size, determine if the amplitude of the unwanted image. If the unwanted image is increasing in amplitude, stop the procedure and try the same adjustment on the other DAC control register. Do this until the image rejection can not be improved through further adjustment of these registers.

It should be noted that LO feedthrough compensation is independent of phase compensation. However, gain compensation could affect the LO compensation because the gain compensation may change the common mode level of the signal. The dc offset of some modulators is common mode level dependent. Therefore it is recommended that the gain adjustment is performed prior to LO compensation.

LO FEEDTHROUGH COMPENSATION

The LO feedthrough compensation is the most complex of all three operations. This is due to the structure of the offset auxiliary DACs as shown in Figure 78. To achieve LO feedthrough compensation in a circuit, each of four outputs of these AUX DACs must be connected through a 50 Ω resistor to ground and through a 250 Ω resistor to one of the four quadrature modulator signal inputs. The purpose of these connections is to drive a very small amount of current into the nodes at the quadrature modulator inputs, therefore adding a slight dc bias to one or the other of the quadrature modulator signal inputs. This can be seen in the schematics for the AD9776A/AD9778A/AD9779A evaluation board (see Figure 107).

To achieve LO feedthrough compensation, the user should start with the default conditions of the AUX DAC sign registers, then increment the magnitude of one or the other AUX DAC output currents. While this is being done, the amplitude of the LO feedthrough at the quadrature modulator output should be sensed. If the LO feedthrough amplitude increases, try either changing the sign of the AUX DAC being adjusted, or try adjusting the output current of the other AUX DAC. It may take practice before an effective algorithm is achieved. Using the AD9776A/AD9778A/AD9779A evaluation board, the LO feedthrough can typically be adjusted down to the noise floor, although this is not stable over temperature.

RESULTS OF GAIN AND OFFSET CORRECTION

The results of gain and offset correction can be seen in Figure 81 and Figure 82. Figure 81 shows the output spectrum of the quadrature demodulator before gain and offset correction. Figure 82 shows the output spectrum after correction. The LO feedthrough spur at 2.1 GHz has been suppressed to the noise level. This result can be achieved by applying the correction, but the correction needs to be repeated after a large change in temperature.

Note that the gain matching improved the negative frequency image rejection, but there is still a significant image present. The remaining image is now due to phase mismatch in the quadrature modulator. Phase mismatch can be distinguished from gain mismatch, by the shape of the image. Note that the image in Figure 81 is relatively flat and the image in Figure 82 slopes down with frequency. Phase mismatch is frequency dependent, so an image dominated by phase mismatch has this sloping characteristic.

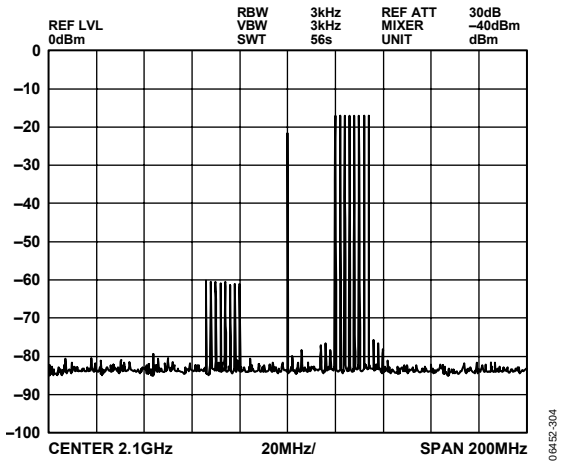


Figure 81. AD9779A and ADL5372 with a Multitone Signal at 2.1GHz, No Gain or LO Compensation

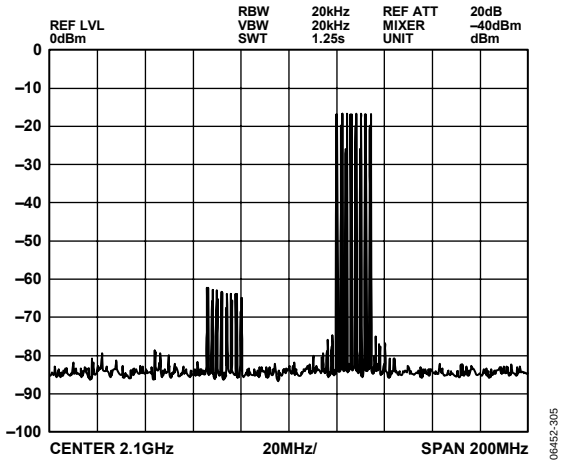


Figure 82. AD9779A and ADL5372 with a Multitone Signal at 2.1 GHz, Gain and LO Compensation Optimized

POWER DISSIPATION

Figure 83 to Figure 91 show the power dissipation of the 1.8 V and 3.3 V digital and clock supplies in single DAC and dual DAC modes. In addition to this, the power dissipation/current of the 3.3 V analog supply (mode and speed independent) in single DAC mode is 102 mW/31 mA. In dual DAC mode, this is 182 mW/55 mA. When the PLL is enabled, it adds 50 mA/90 mW to the 1.8 V clock supply.

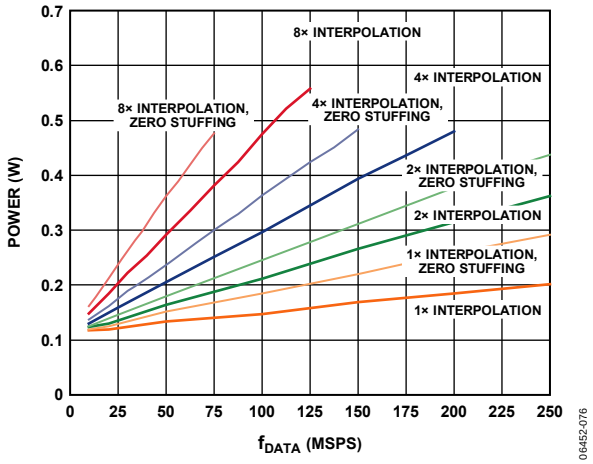


Figure 83. Total Power Dissipation, I Data Only, Real Mode

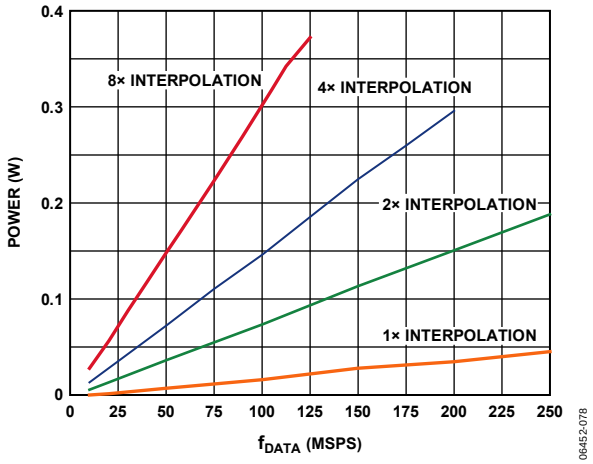


Figure 84. Power Dissipation, Digital 1.8 V Supply, I Data Only, Real Mode, Does Not Include Zero Stuffing

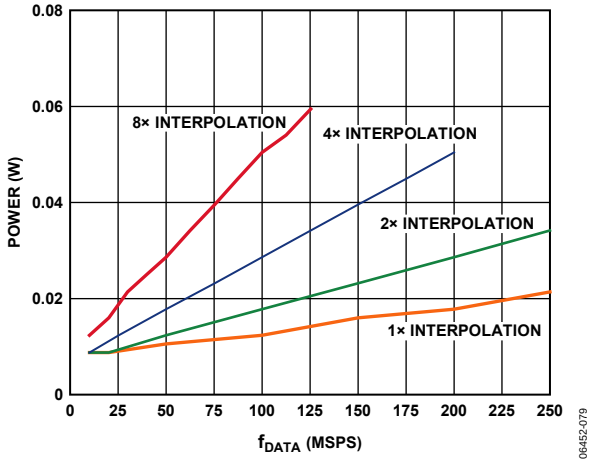


Figure 85. Power Dissipation, Clock 1.8 V Supply, I Data Only, Real Mode, Includes Modulation Modes, Does Not Include Zero Stuffing

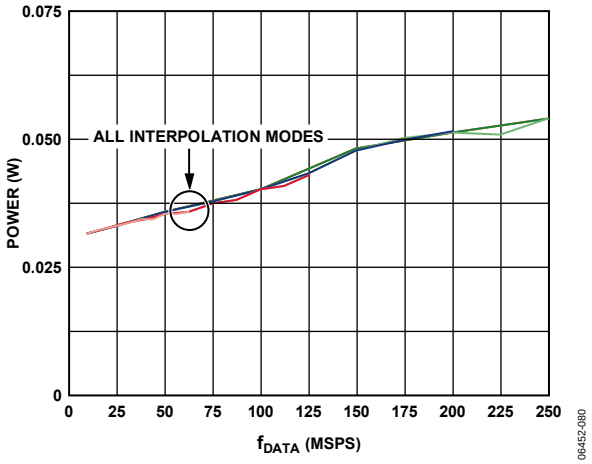


Figure 86. Power Dissipation, Digital 3.3 V Supply, I Data Only, Real Mode, Includes Modulation Modes and Zero Stuffing

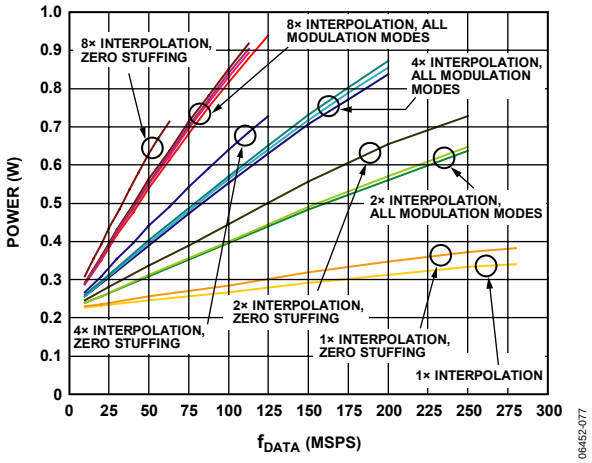


Figure 87. Total Power Dissipation, Dual DAC Mode

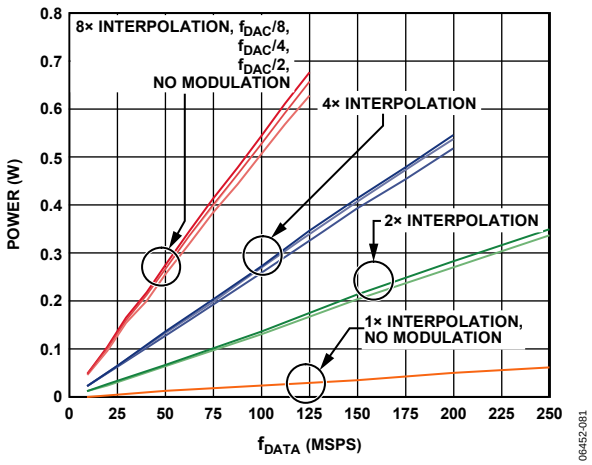


Figure 88. Power Dissipation, Digital 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

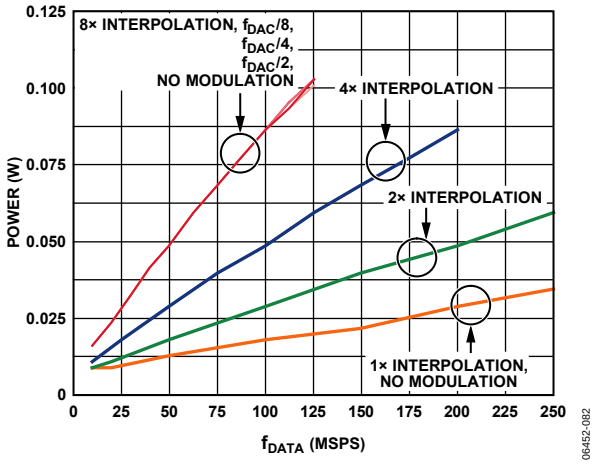


Figure 89. Power Dissipation, Clock 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

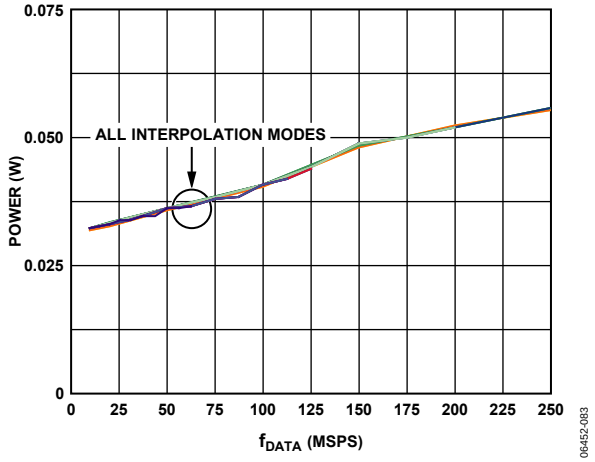


Figure 90. Power Dissipation, Digital 3.3 V Supply, I and Q Data, Dual DAC Mode

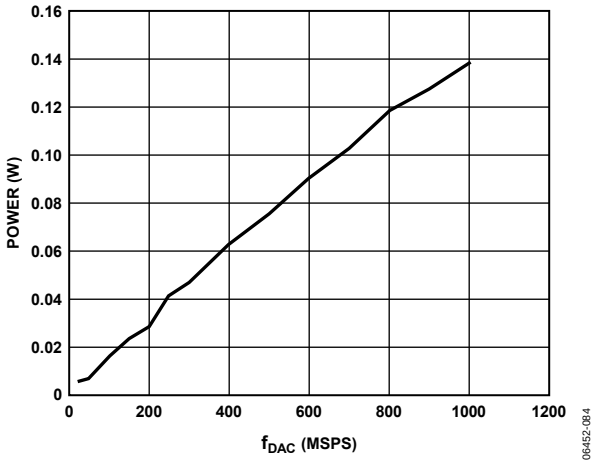


Figure 91. DVDD18 Power Dissipation of Inverse Sinc Filter

POWER-DOWN AND SLEEP MODES

The AD9776A/AD9778A/AD9779A have a variety of power-down modes, so that the digital engine, main TxDACs, or auxiliary DACs can be powered down individually or together. Via the SPI port, the main TxDACs can be placed in sleep or power-down mode. In sleep mode, the TxDAC output is turned off, thus reducing power dissipation. The reference remains powered on, however, so that recovery from sleep mode is very fast. With the power-down mode bit set (Register 0x00, Bit 4), all analog and digital circuitry, including the reference, is powered down. The SPI port remains active in this mode. This mode offers more substantial power savings than sleep mode, but the turn-on time is much longer. The auxiliary DACs also have the capability to be programmed into sleep mode via the SPI port. The auto power-down enable bit (Register 0x00, Bit 3) controls the power-down function for the digital section of the devices. The auto power-down function works in conjunction with the TXENABLE pin (Pin 39) according to the following:

TXENABLE (Pin 39) =

0: autopower-down enable =
0: flush data path with 0s
1: flush data for multiple REFCLK cycles; then automatically place the digital engine in power-down state. DACs, reference, and SPI port are not affected.

or TXENABLE (Pin 39) =

1: normal operation.

As shown in Figure 92, the power dissipation saved by using the power-down mode is nearly proportional to the duty cycle of the signal at the TXENABLE pin.

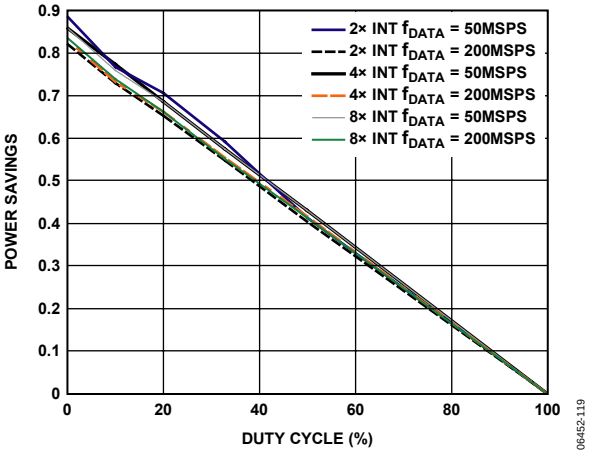


Figure 92. Power Savings Based on Duty Cycle of TXENABLE

If the TxEnable Invert bit (Register 0x02, Bit 1) is set, the function of this TXENABLE pin is inverted.

INTERLEAVED DATA MODE

The TxEnable bit is a dual functioning bit. In dual port mode, it is simply used to power down the digital section of the devices. In interleaved mode, TxEnable acts as an IQSELECT signal and indicates to which DAC the P1D data is targeted. The IQSELECT signal should be time aligned with the input data. When IQSELECT is high the corresponding data-word is sent to the I DAC and when IQSELECT is low the corresponding data is sent to the Q DAC. The timing of the digital interface in interleaved mode is shown in Figure 93.

The Q First bit (Register 0x02, Bit 0) controls the pairing order of the input data. With the Q First bit set to the default of 0, the IQ pairing sent to the DACs is the two input data words corresponding to IQSELECT low followed by IQSELECT high. With Q First set to 1, the IQ pairing sent to the DACs is the two input data-words corresponding to IQSELECT high followed by IQSELECT low. Note that with Q First set, the I data still corresponds to the IQSELECT high word and the Q data corresponds to the IQSELECT low word and only the pairing changes.

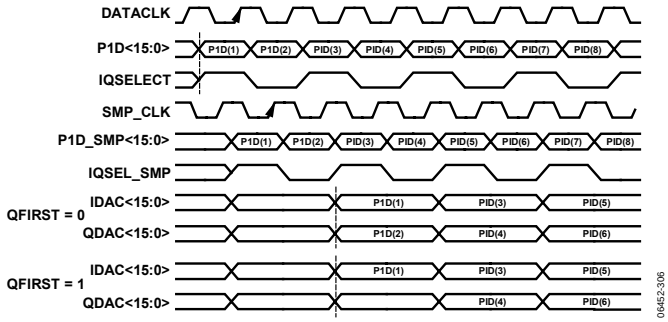


Figure 93. Interleaved Mode Digital Interface Timing

If TXENABLE is brought low and held low for multiple REFCLK cycles, then the devices flush the data in the interpolation filters, and shut down the digital engine after the filters are flushed. The number of REFCLK cycles it takes to go into this power-down mode is a function of the length of the equivalent 2×, 4×, or 8× interpolation filter.

TIMING INFORMATION

Figure 94 to Figure 97 show some of the various timing possibilities when the PLL is enabled. The combination of the settings of N_2 and N_3 from Figure 74 means that the reference clock frequency (f_{REFCLK}) can be a multiple of the actual input data rate. Figure 94 to Figure 97 show what the timing looks like when $N_2/N_3 = 1$ ($N_2 = N_3$ = interpolation rate).

In interleaved mode, set up and hold times of DATACLK out with respect to the data inputs are the same as those shown in Figure 94 to Figure 97. It is recommended that any toggling of TXENABLE occur concurrently with the digital data input transitions. In this way, timing margins between DATACLK, TXENABLE, and digital input data are optimized.

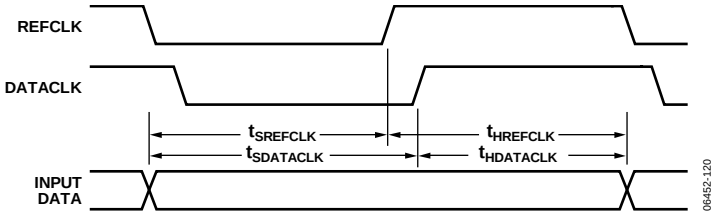


Figure 94. Timing Specifications, PLL Enabled or Disabled, Interpolation = 1×

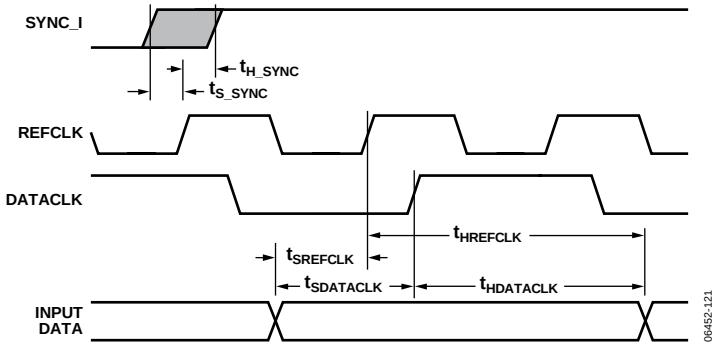


Figure 95. Timing Specifications, PLL Enabled or Disabled, Interpolation = 2×

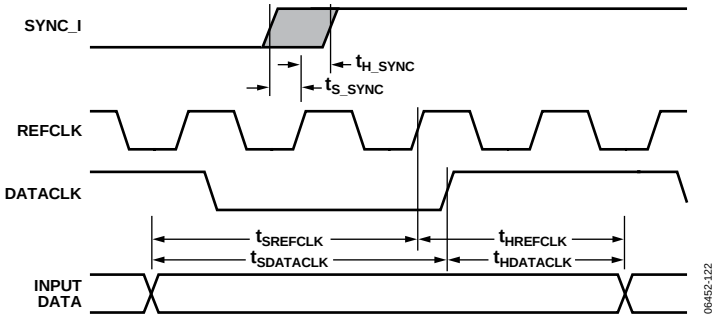


Figure 96. Timing Specifications, PLL Enabled or Disabled, Interpolation = 4×

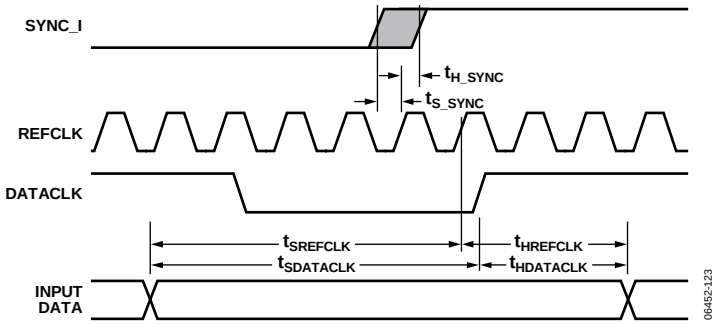


Figure 97. Timing Specifications, PLL Enabled or Disabled, Interpolation = 8×

See Table 20 for specifications of the drift of input data set up and hold time vs. temperature, as well as the data keep out window (KOW). Note that although these specifications do drift, the length of the keep out window, where input data is invalid, changes very little over temperature.

Table 20. AD9776A/AD9778A/AD9779A Timing Specifications vs. Temperature

Timing Parameter	Temperature	Min t_S (ns)	Min t_H (ns)	Max KOW (ns)
DATA with respect to REFCLK±	−40°C	−0.8	3.35	2.55
	+25°C	−1.0	3.5	2.5
	+85°C	−1.1	3.8	2.7
	−40°C to +85°C	−0.8	3.8	3.0
DATA with respect to DATACLK	−40°C	2.5	−0.05	2.45
	+25°C	2.7	−0.2	2.5
	+85°C	3.0	−0.4	2.6
	−40°C to +85°C	3.0	−0.05	2.95
SYNC_I± to REFCLK±	−40°C	0.3	0.65	0.95
	+25°C	0.25	0.75	1.0
	+85°C	0.15	0.90	1.05
	−40°C to +85°C	0.3	0.90	1.2

TIMING VALIDATION OF DIGITAL INPUT DATA BUS

Synchronizing the input data bus for valid timing is achieved by meeting the timing relationships between the digital input data to REFCLK and DATA out specified in Table 20. If the user is synchronizing the input data to the DATACLK (Pin 37), the SYNC_I input signal does not need to be applied and can be ignored (connect to GND).

SYNCHRONIZATION OF INPUT DATA TO REFCLK INPUT (PIN 5 AND PIN 6) WITH PLL ENABLED OR DISABLED

Synchronizing the input data bus to the REFCLK input requires the use of the SYNC_I input pins (Pin 13 and Pin 14). If the SYNC_I input is not used, there is a phase ambiguity between the DATACLK output and the REFCLK input. This ambiguity is directly related to the interpolation rate in which the AD9776A/AD9778A/AD9779A are currently operating. Because input data is latched on the rising edge of DATACLK, it is impossible for the user to determine on which of multiple internal DACCLK edges (as an example, one of four edges in 4× interpolation) the input data actually latches. For the user to specifically determine the exact edge of the internal DACCLK on which the data is being latched, a rising edge must be periodically applied to SYNC_I. The frequency of the SYNC_I signal must be equal to $f_{DAC}/2^N$, N being an integer, and must be no greater than the frequency of DATACLK for proper synchronization. There is no limit on how slow the SYNC_I signal can be driven. As long as the setup and hold timing relationship between SYNC_I and REFCLK given in Table 20 is met, the input data is latched on the immediate next rising edge of REFCLK. Note that a rising edge of DATACLK occurs concurrently with the next REFCLK rising edge, after a short propagation delay. Although this propagation delay is not specified, input data setup and hold timing information is given with respect to REFCLK and DATACLK in Figure 94 to Figure 97. Also note that in 1× interpolation, because there is no phase ambiguity, there is no need to use the SYNC_I signal.

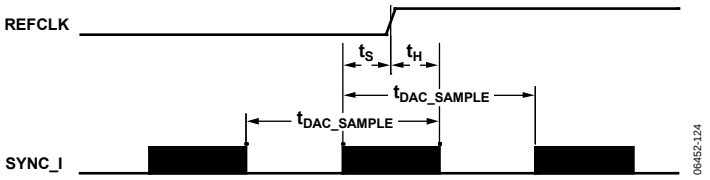


Figure 98. Valid Timing Relationship for SYNC_I to REFCLK

VALID TIMING WINDOW, SYNC_I TO REFCLK AND TO INTERNAL DACCLK

In addition to the timing requirements of SYNC_I with respect to REFCLK, it is important to understand that the valid timing window for SYNC_I is limited by the internal DAC sample rate (see Figure 98). When the t_S and t_H requirements are met, the valid timing window for SYNC_I extends only as far as one period of the internal DAC sample rate (minus t_S and t_H). Failure to meet this timing specification can possibly result in erroneous data being latched into the AD9776A/AD9778A/AD9779A digital inputs.

As an example, if the AD9776A/AD9778A/AD9779A input data rate is 122.88 MSPS and the REFCLK is the same, with the AD9776A/AD9778A/AD9779A in 4× interpolation, t_{DAC_SAMPLE} is 1/491.52 MHz or about 2 ns. With a t_S of −0.2 ns and t_H of +1.0 ns, this gives a valid timing window for SYNC_I of

2 ns − 0.8 ns = 1.2 ns

Also, the timing window of the digital input data to REFCLK can be moved in increments of one internal DACCLK cycle by using the DAC clock offset register (Register 0x07 Bits<4:0>).

Because SYNC_I can be run at the same frequency as REFCLK when the PLL is enabled, it is highly recommend that in this condition, that REFCLK and SYNC_I originate from the same source. This limits the variation in time between these two signals and makes the overall timing budget easier to achieve. A slight delay may be necessary on the REFCLK path in this configuration to add more timing margin between REFCLK and SYNC_I (see Table 20 for timing relationships).

Using Data Delay to Meet Timing Requirements

To meet strict timing requirements at input data rates of up to 300 MSPS, the AD9776A/AD9778A/AD9779A have a fine timing feature. Fine timing adjustments are made by programming values into the data clock delay register (Register 0x04, Bits<7:4>) and Register 0x01 Bit 1. This register can be used to add delay between the REFCLK input and the DATACLK output. Figure 99 shows the default delay present when DATACLK delay is disabled. The DATACLK delay enable bit is found in Register 0x02, Bit 4. Figure 100 shows the delay present when DATACLK delay is enabled and set to 00000. Figure 101 indicates the delay when DATACLK delay is enabled and set to 01111. Note that the setup and hold times specified for data to DATACLK are defined for DATACLK delay disabled.

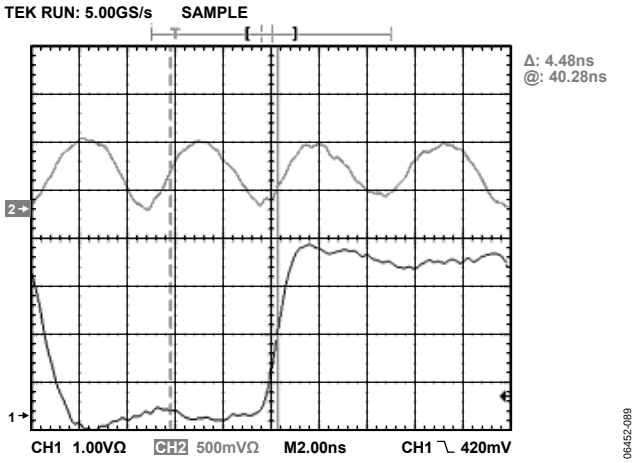


Figure 99. Delay from REFCLK to DATACLK with DATACLK Delay Disabled

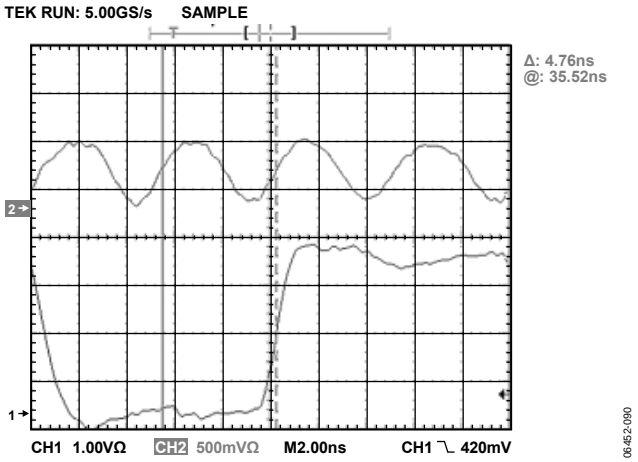


Figure 100. Delay from REFCLK to DATACLK Out with DATACLK Delay = 00000

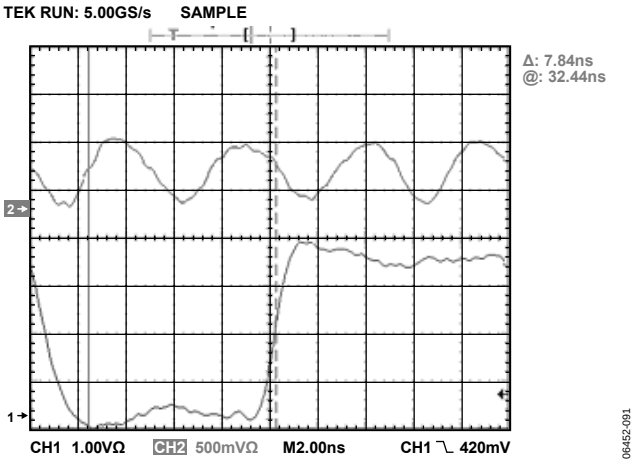


Figure 101. Delay from REFCLK to DATACLK Out with DATACLK Delay = 01111

The difference between the minimum delay shown in Figure 100 and the maximum delay shown in Figure 101 is the range programmable via the DATACLK delay register. The delay (in absolute time) when programming DATACLK delay between 0000 and 1111 is a linear extrapolation between these two figures. The typical delays per increment over temperature are shown in Table 21.

Table 21. Data Delay Line Typical Delays Over Temperature

Delay	−40°C	+25°C	+85°C	Unit
Delay Between Disabled and Enabled	630	700	740	ps
Average Delay per Increment	175	190	210	ps

The frequency of DATACLK output depends on several programmable settings. Interpolation, zero stuffing, and input mode (see Table 22) all have an effect on the REFCLK frequency. The divisor function between REFCLK and DATACLK is equal to the values shown in Table 22.

Table 22. REFCLK to DATACLK Divisor Ratio

Interpolation	Zero Stuffing	Input Mode	Divisor
1	Disabled	Dual port	1
2	Disabled	Dual port	2
4	Disabled	Dual port	4
8	Disabled	Dual port	8
1	Disabled	Interleaved	Invalid
2	Disabled	Interleaved	1
4	Disabled	Interleaved	2
8	Disabled	Interleaved	4
1	Enabled	Dual port	2
2	Enabled	Dual port	4
4	Enabled	Dual port	8
8	Enabled	Dual port	16
1	Enabled	Interleaved	1
2	Enabled	Interleaved	2
4	Enabled	Interleaved	4
8	Enabled	Interleaved	8

In addition to this divisor function, DATACLK can be divided by up to an additional factor of 4, according to the state of the DATACLK divide register (Register 0x03, Bits<5:4>). For more details, see Table 23.

The maximum divisor resulting from the combination of the values in Table 22, and the DATACLK divide register is 32.

Table 23. Extra DATACLK Divider Ratio

Register 0x03, Bits<5:4>	Divider Ratio
00	1
01	2
10	4
11	1

DATA DELAY LINE, ERROR CORRECTION, MANUAL MODE

As shown in Figure 99, Figure 100, and Figure 101, the DATACLK delay setting allows the user to adjust the timing relationship between DATACLK output and the input data. This provides the user flexibility as it allows the timing relationship of the input data to the DATACLK output to be programmed via the SPI port. In addition to simply programming the data clock delay for a given value, the AD9776A/AD9778A/AD9779A also allow the user, via SPI readback and a programmable timing margin, to determine to a good degree of accuracy how close the present timing is to an invalid region. Note that because this feature adds delay to the DATACLK output (not the input data path) signal, it has no effect on the timing relationship between the input data and REFCLK.

With the error correction enabled in manual mode (Register 3, Bit 7 = 0), the user can set a timing margin window and then sweep the DATACLK delay (described previously). The full span of the delay is equal to about 5.6 ns in 32 increments, so is about 180 ps/increment as shown in Table 21. The amount of timing margin that can be set is only four bits (Register 3, Bits<3:0>), but has the same amount per increment as the DATACLK delay, roughly 180 ps/increment. Internally, a sampling clock samples the digital input data, and can sense a transition on the data inputs. If a data transition is sensed that is close to the latching DATACLK edge, then a Data Delay IRQ is generated that can be read from the SPI port Register 19, Bit 7.

This bit must be enabled by Register 0x19, Bit 3. The sense of Bit 4 of this same register can be used to determine whether the IRQ is indicating possible set up or hold violation. The Data Delay IRQ can also be sensed at an external pin (Pin 71). The internal SYNC IRQ and DATA DELAY IRQ functions are OR'ed together at Pin 71 so that an IRQ from either source sets this pin low. The IRQ does not differentiate between setup and hold errors so that a full sweep of DATACLK delay may be necessary to determine which of these two possibilities is causing the IRQ generation. The margin around the data transition which the internal circuitry is sensitive to can be adjusted by the window

detect setting in the SPI register (Register 3, Bits<3:0>). IRQ is set when the timing margin between the input data and DATACLK out (minus the programmable margin) violates the setup and hold times given in Table 20. Improvement in setup time can therefore be achieved by reducing the DATACLK delay, and improvement in hold time can be achieved by increasing DATACLK delay. Also, note that if an IRQ is set, it does not reset itself if the IRQ fault is resolved. To reset the IRQ, a 0 must be written to the IRQ register.

DATA DELAY LINE, ERROR CORRECTION AUTO MODE

The data delay error correction can also be run in an automatic mode where the AD9776A/AD9778A/AD9779A determines the optimal timing and set the data delay accordingly. The value in the DATA DELAY register can then be read back by the user if necessary. In auto mode, the timing margin window must still be programmed by the user.

In operation, the autotiming mode can be left on and tracks with temperature with no other user intervention.

MULTIPLE DAC SYNCHRONIZATION

The AD9776A/AD9778A/AD9779A have programmable features that allow the CMOS digital data bus inputs and internal filers on multiple devices to be synchronized. This means that the DATACLK output signal on an AD9776A/AD9778A/AD9779A can be used to register the output data for a data bus delivering data to multiple AD9776A/AD9778A/AD9779As. The details of this operation are given in Analog Devices Application Note AN-822.

EVALUATION BOARD OPERATION

The AD9776A/AD9778A/AD9779A evaluation board is designed to optimize the DAC performance and the speed of the digital interface, yet remains user friendly. To operate the board, the user needs a power source, a clock source, and a digital data source. The user also needs a spectrum analyzer or an oscilloscope to look at the DAC output. The diagram in Figure 102 illustrates the test setup. A sine or square wave clock works well as a clock source. The dc offset on the clock is not a problem, because the clock is ac-coupled on the evaluation board before the REFCLK inputs. All necessary connections to the evaluation board are shown in more detail in Figure 103.

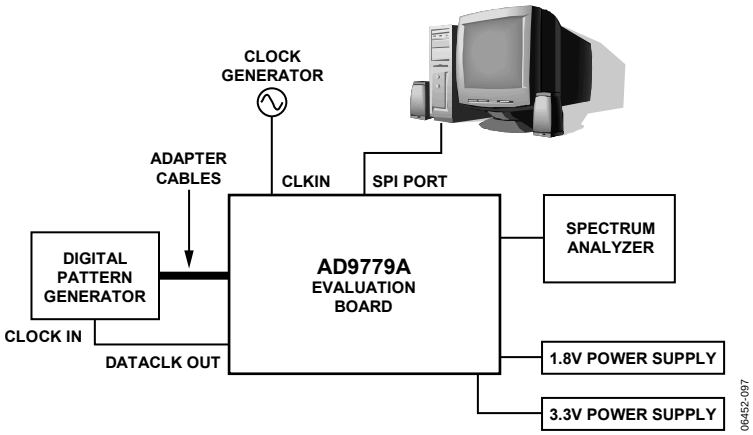


Figure 102. Typical Test Setup

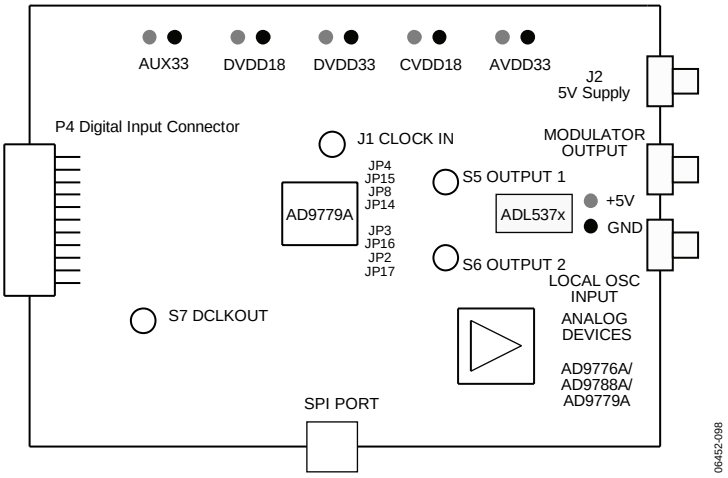


Figure 103. AD9776A/AD9778A/AD9779A Evaluation Board Showing All Connections

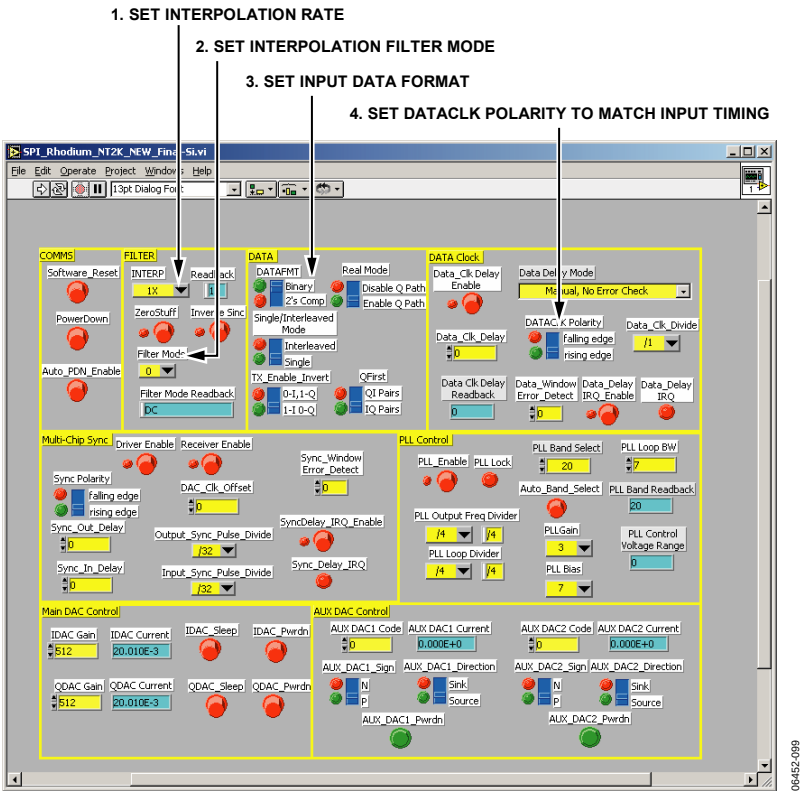


Figure 104. SPI Port Software Window

The evaluation board comes with software that allows the user to program the SPI port. Via the SPI port, the devices can be programmed into any of its various operating modes. When first operating the evaluation board, it is useful to start with a simple configuration, that is, a configuration in which the SPI port settings are as close as possible to the default settings. The default software window is shown in Figure 104. The arrows indicate which settings need to be changed for an easy first time evaluation. Note that this implies that the PLL is not being used and that the clock being used is at the speed of the DAC output sample rate. For a more detailed description of how to use the PLL, see the PLL Loop Filter Bandwidth section.

The default settings for the evaluation board allow the user to view the differential outputs through a transformer that converts the DAC output signal to a single-ended signal. On the evaluation board, these transformers are designated T1A, T2A, T3A, and T4A. There are also four common-mode transformers on the board that are designated T1B, T2B, T3B, and T4B. The recommended operating setup places the transformer and common-mode transformer in series. A pair of transformers and common-mode transformers are installed on each DAC output, so that the pairs can be set up in either order. As an example, for the frequency range of dc to 30 MHz, it is recommended that the transformer be placed right after the DAC. Above DAC output frequencies of 30 MHz, it is recommended that the common-mode transformer is placed right after the DAC outputs, followed by the transformer.

MODIFYING THE AD9776A/AD9778A/AD9779A EVALUATION BOARD TO USE THE ADL5372 ON-BOARD QUADRATURE MODULATOR

The evaluation board contains an Analog Devices ADL5372 quadrature modulator. The AD9776A/AD9778A/AD9779A and ADL5372 provide an easy-to-interface DAC/modulator combination that can be easily characterized on the evaluation board. Solderable jumpers can be configured to evaluate the single-ended or differential outputs of the AD9776A/AD9778A/AD9779A. This is the default configuration from the factory and consists of the following jumper positions:

JP2, JP3, JP4, JP8—unsoldered
JP14, JP15, JP16, JP17—soldered

To evaluate the ADL5372 on this board, these same jumper positions should be reversed so that they are in the following positions:

JP2, JP3, JP4, JP8—soldered
JP14, JP15, JP16, JP17—unsoldered

Note that the ADL5372 also requires its own separate +5 V and GND connection on the evaluation board.

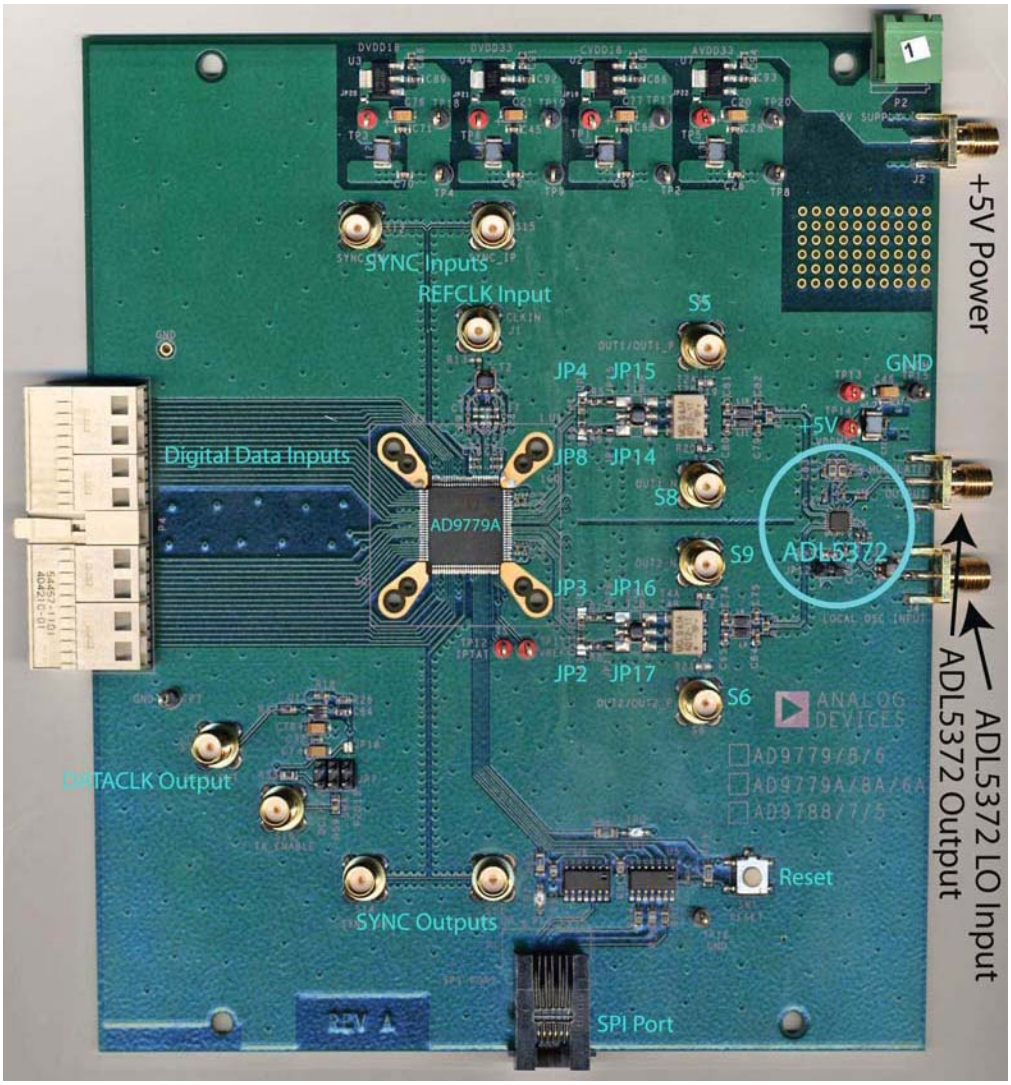


Figure 105. AD9776A/AD9778A/AD9779A Evaluation Board

EVALUATION BOARD SCHEMATICS

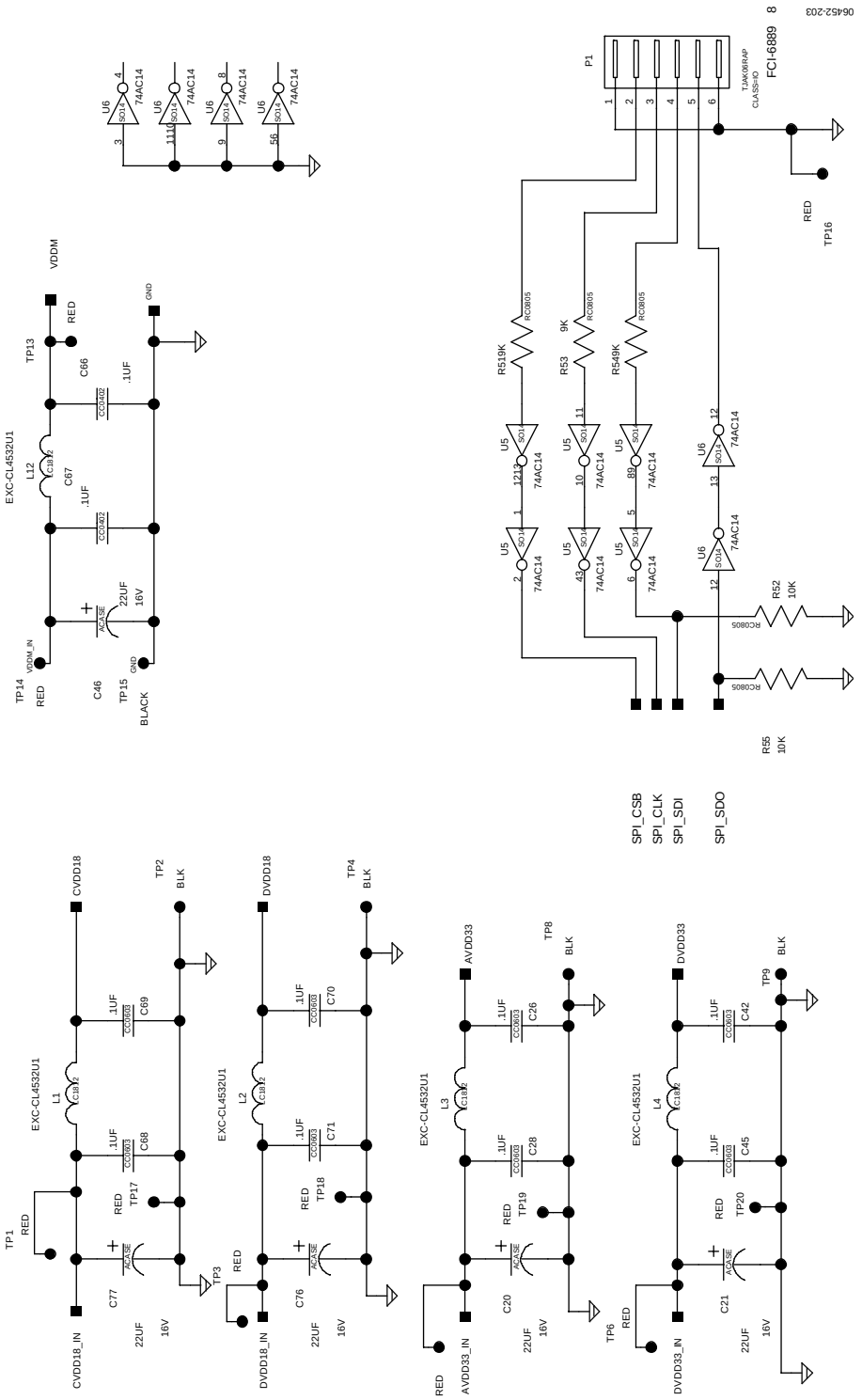


Figure 106. Evaluation Board, Rev. A, Power Supply and Decoupling

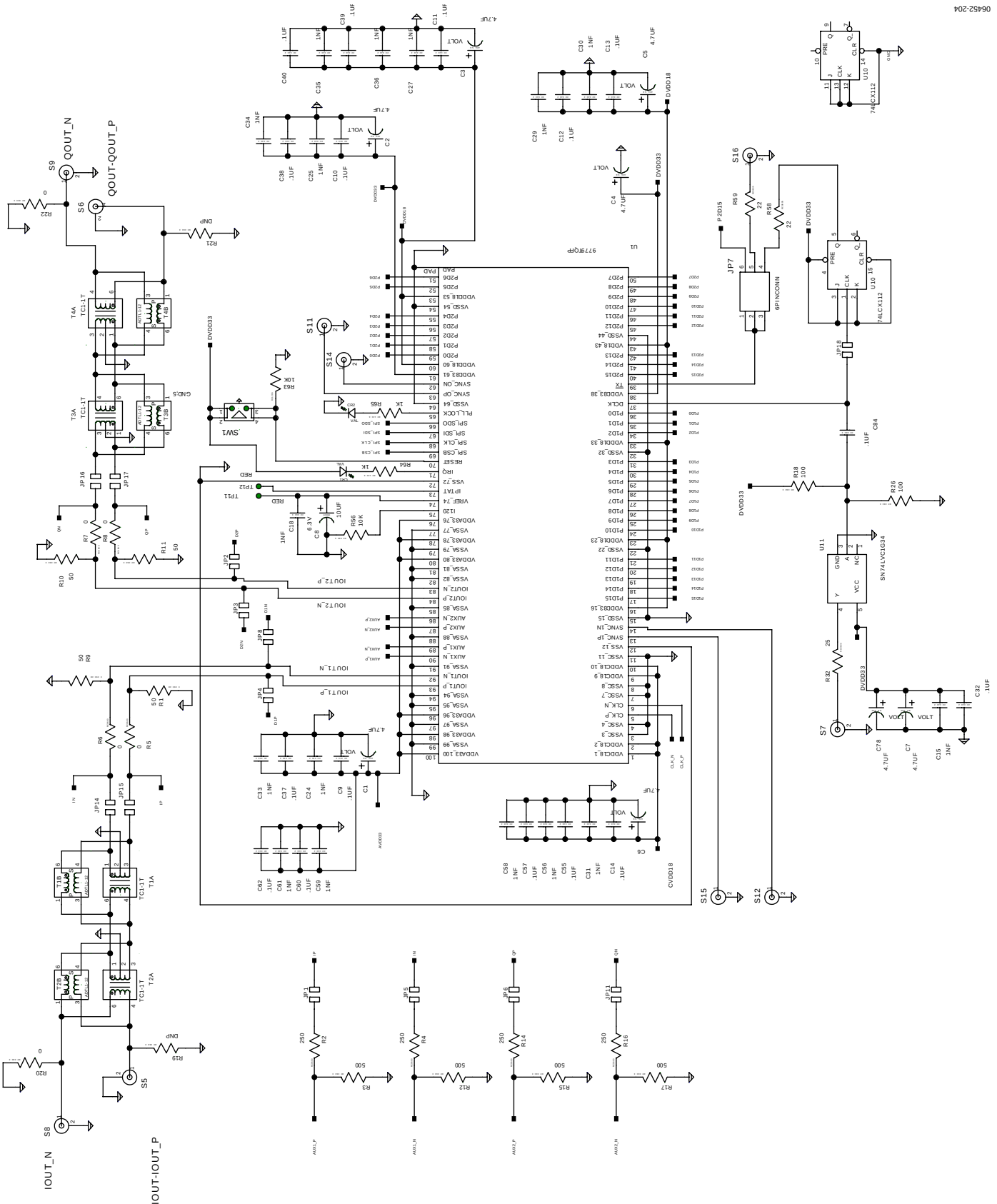


Figure 107. Evaluation Board, Rev. A, Analog and Digital Interfaces to TxDAC

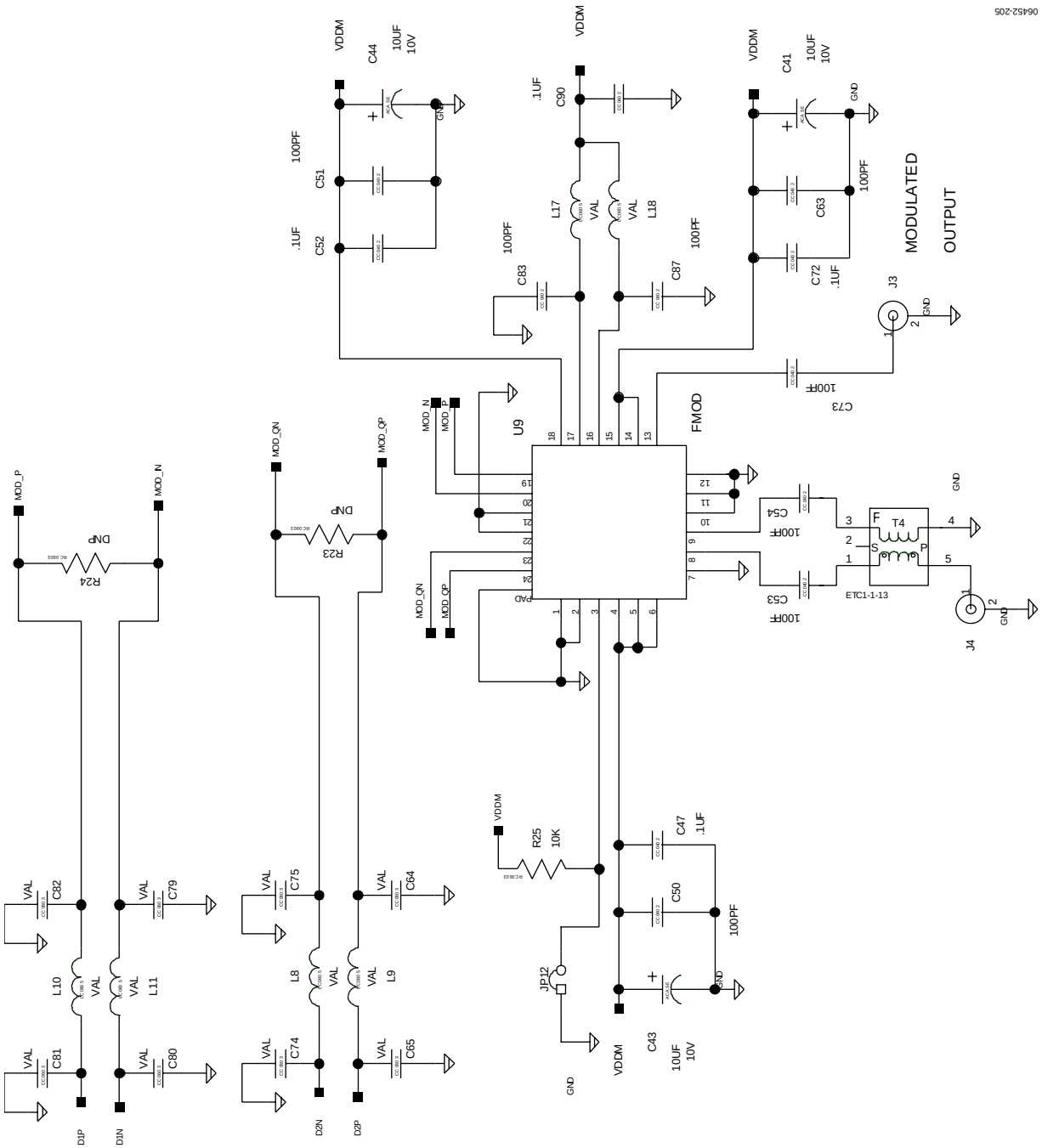


Figure 108. Evaluation Board, Rev. A, ADL5372 (FMOD2) Quadrature Modulator

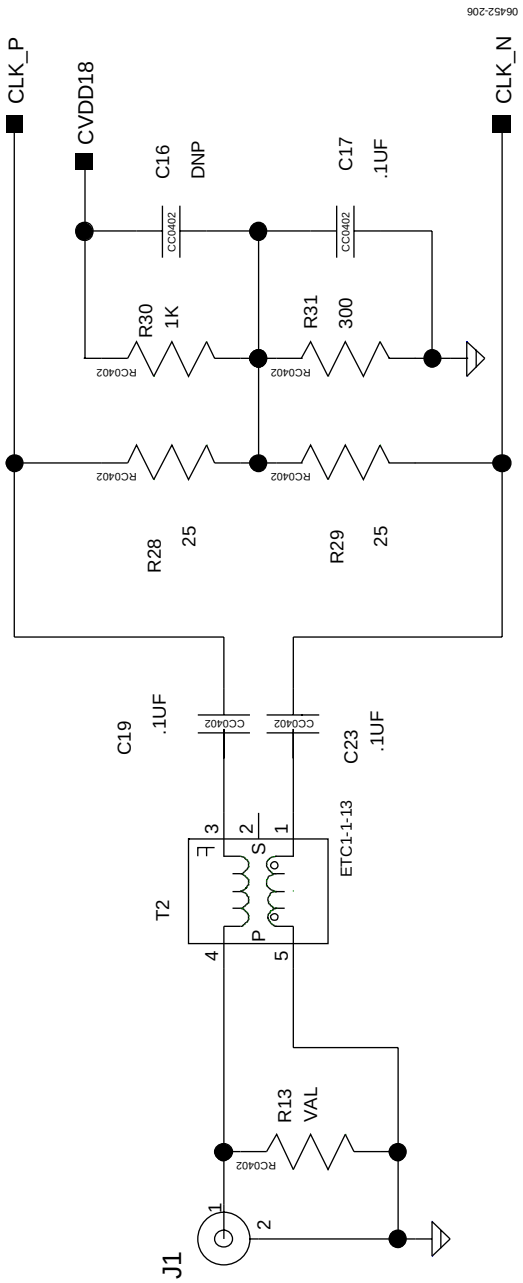


Figure 109. Evaluation Board, Rev. A, Tx DAC Clock Interface

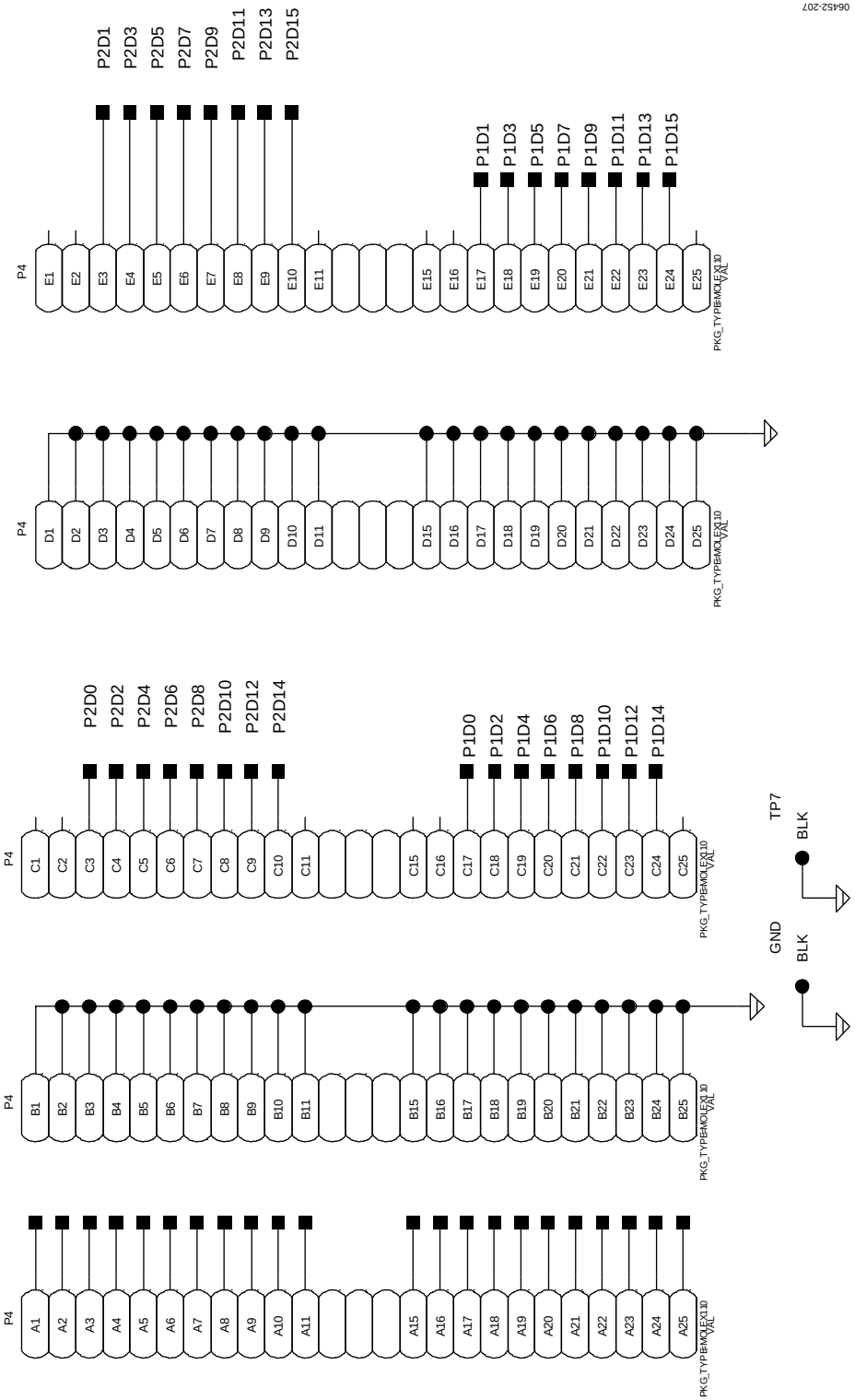


Figure 110. Evaluation Board, Rev. A, Digital Input Data Lines

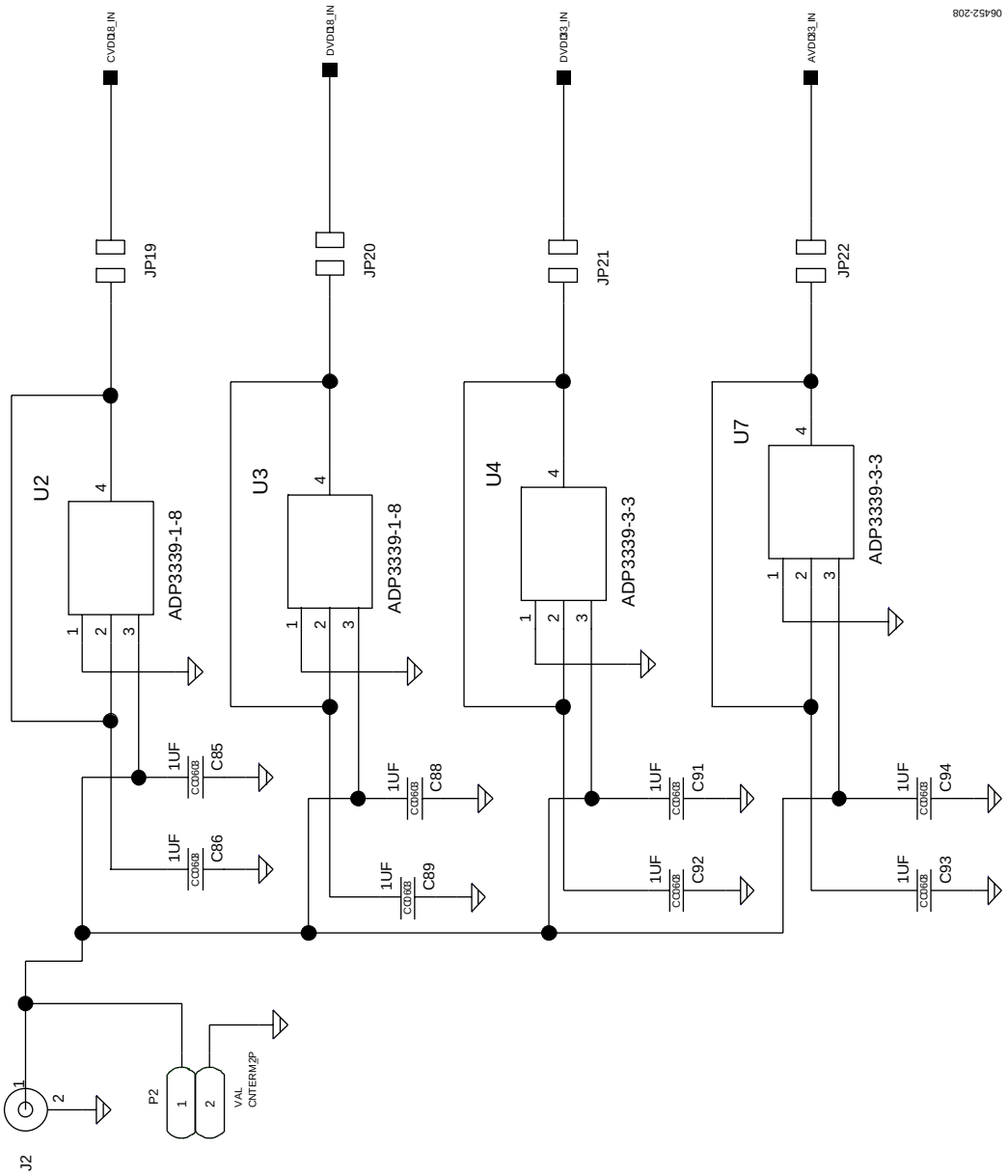


Figure 111. Evaluation Board, Rev. A, On-Board Power Supply

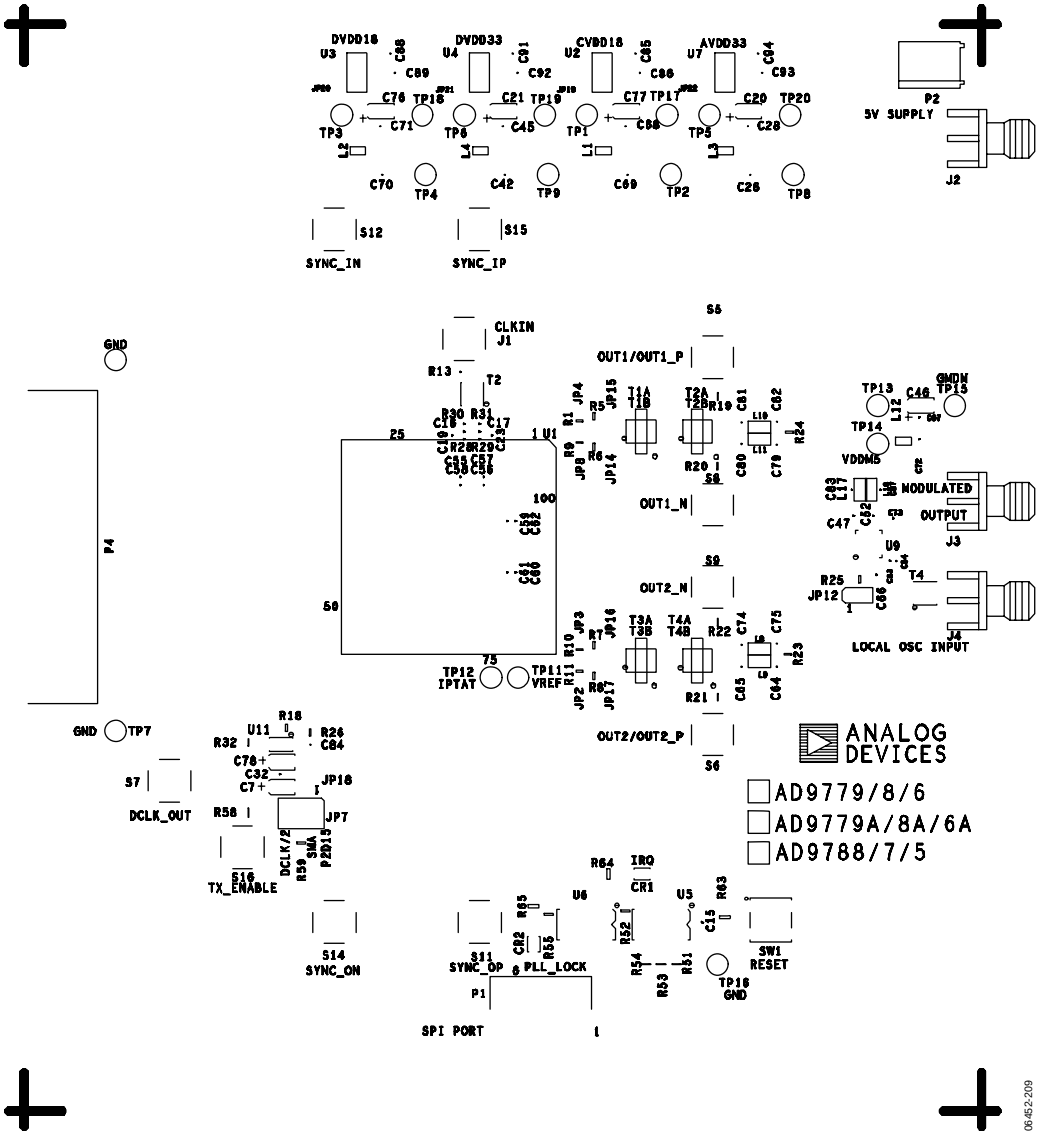


Figure 112. Evaluation Board, Rev A, Top Side Silk Screen

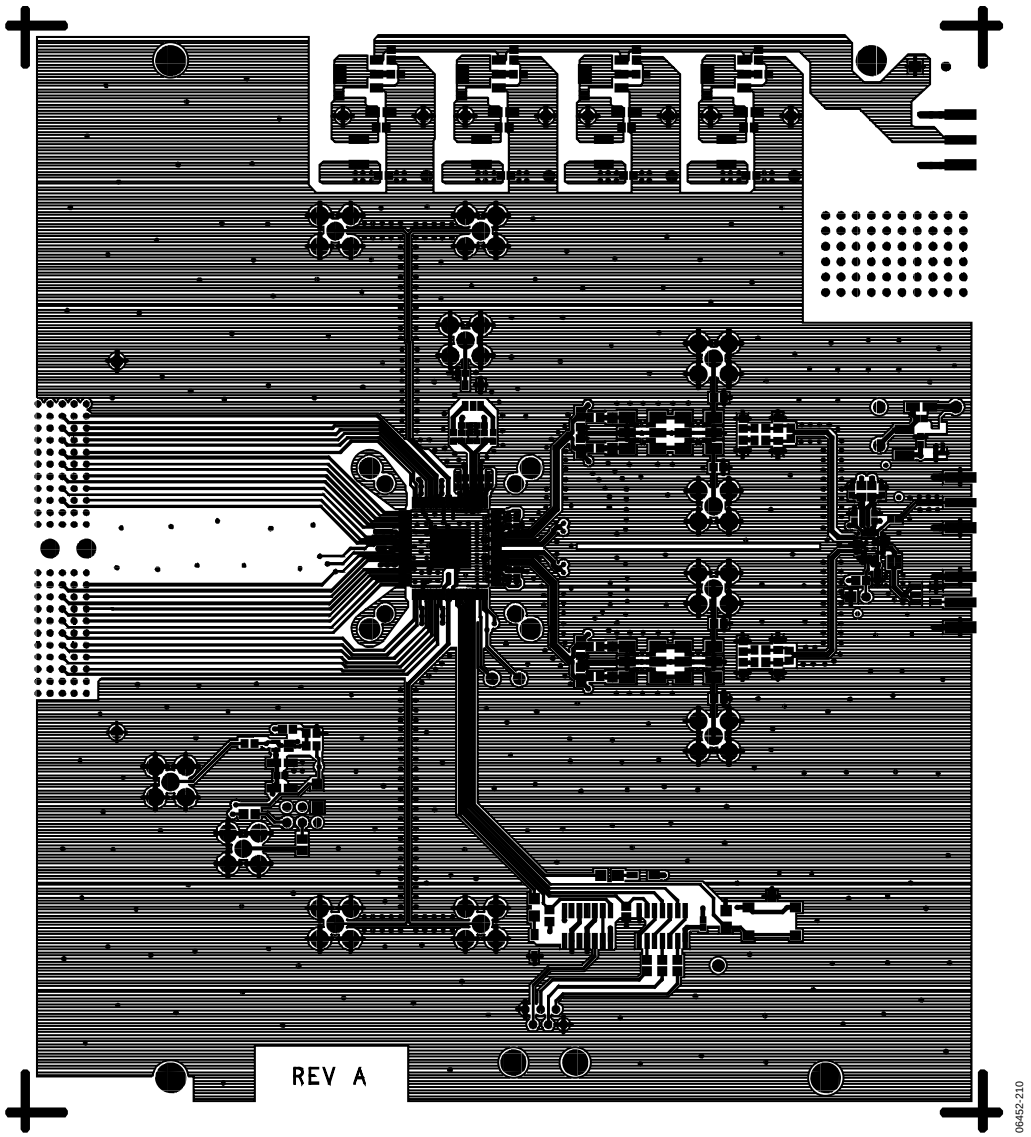


Figure 113. Evaluation Board, Rev. A, Layer 1 (Top Layer)

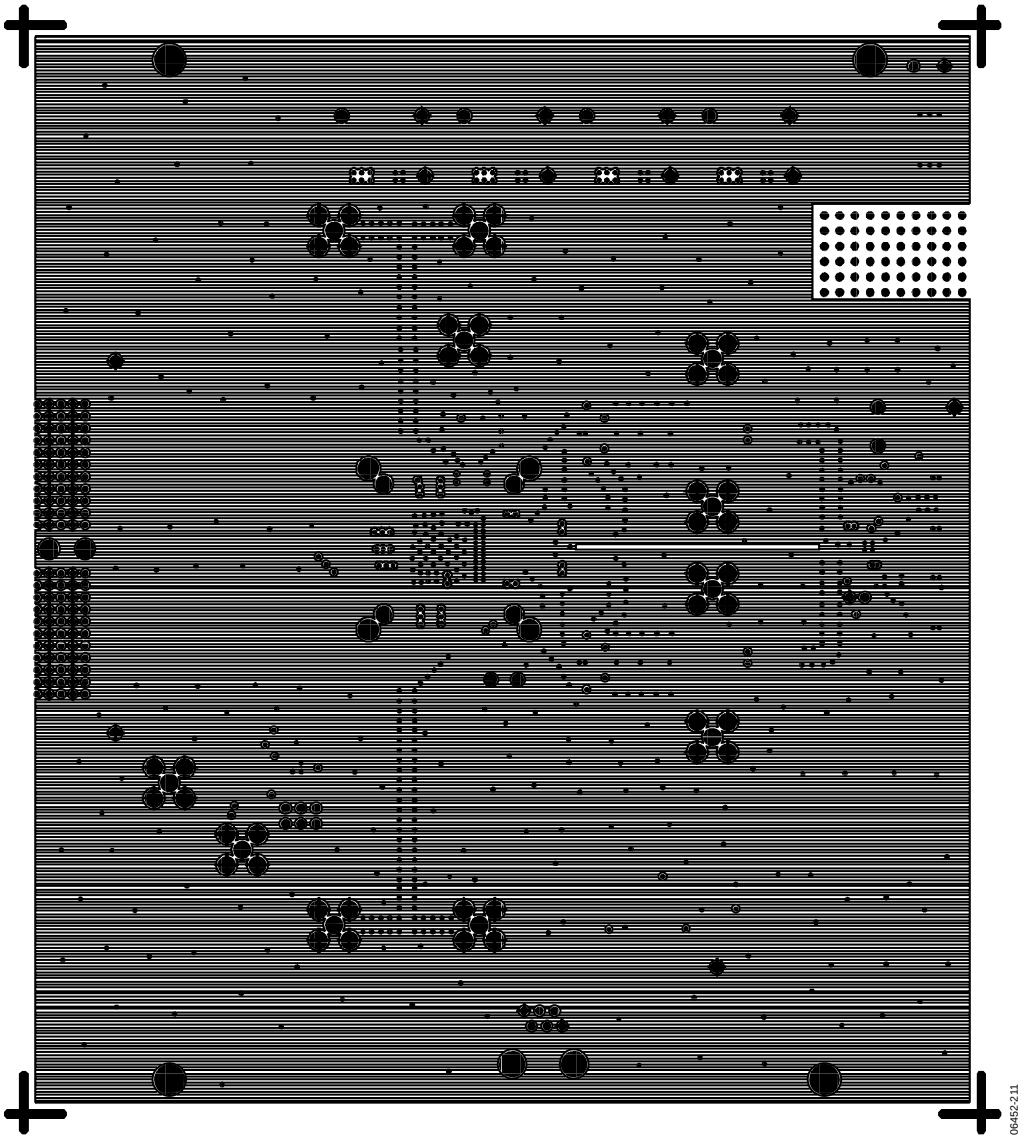


Figure 114. Evaluation Board, Rev. A, Layer 2 (Ground)

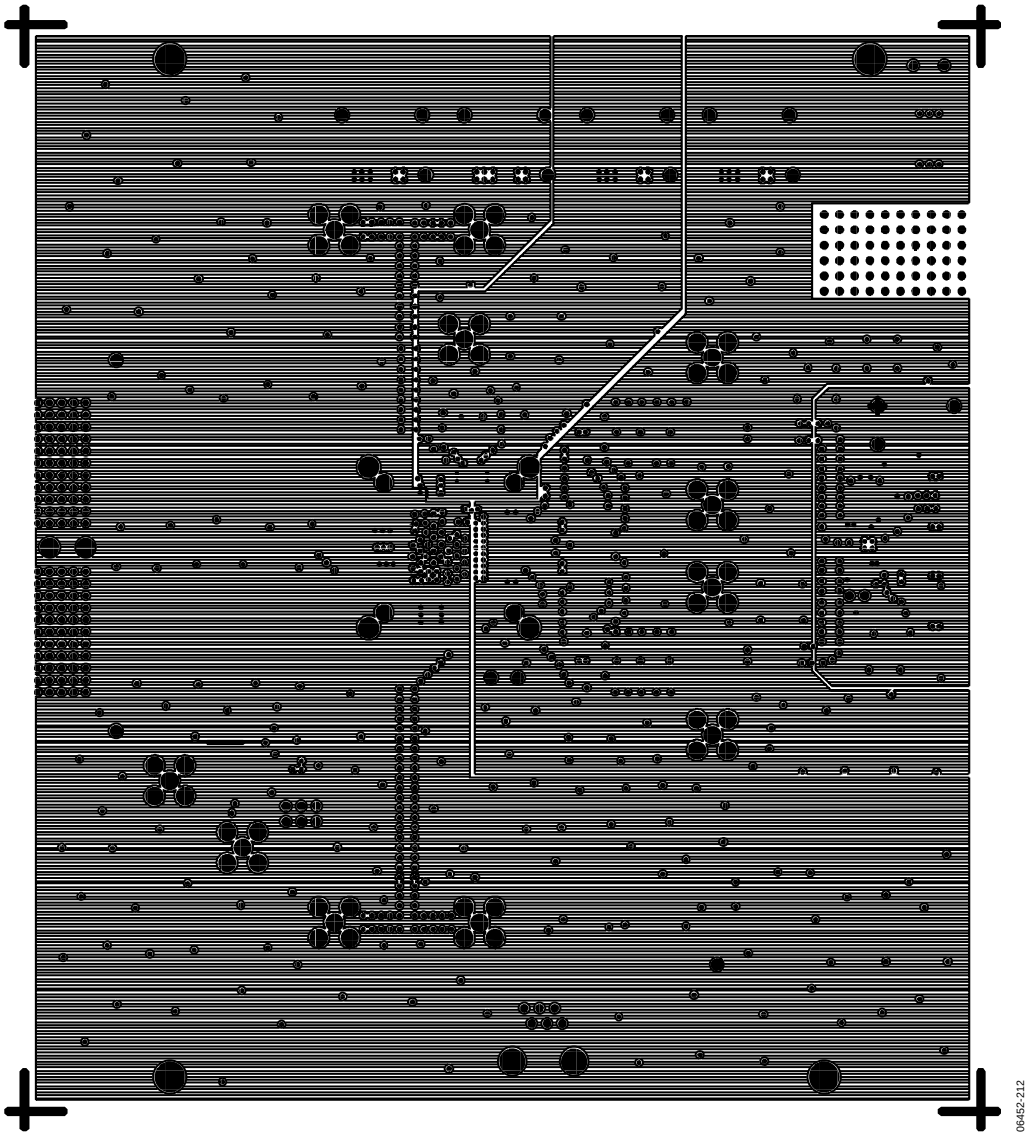


Figure 115. Evaluation Board, Rev. A, Layer 3 (Power)

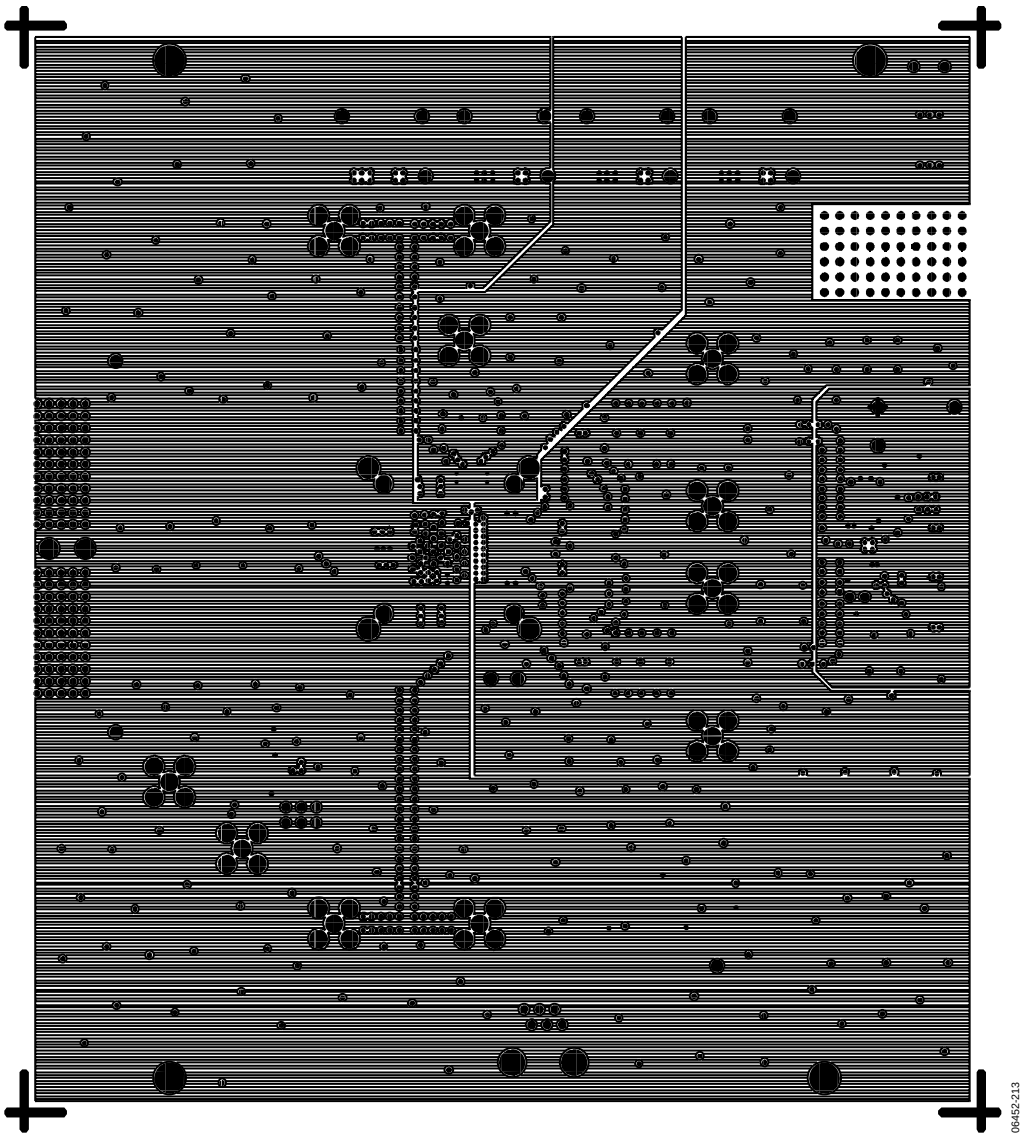


Figure 116. Evaluation Board, Rev. A, Layer 4 (Power)

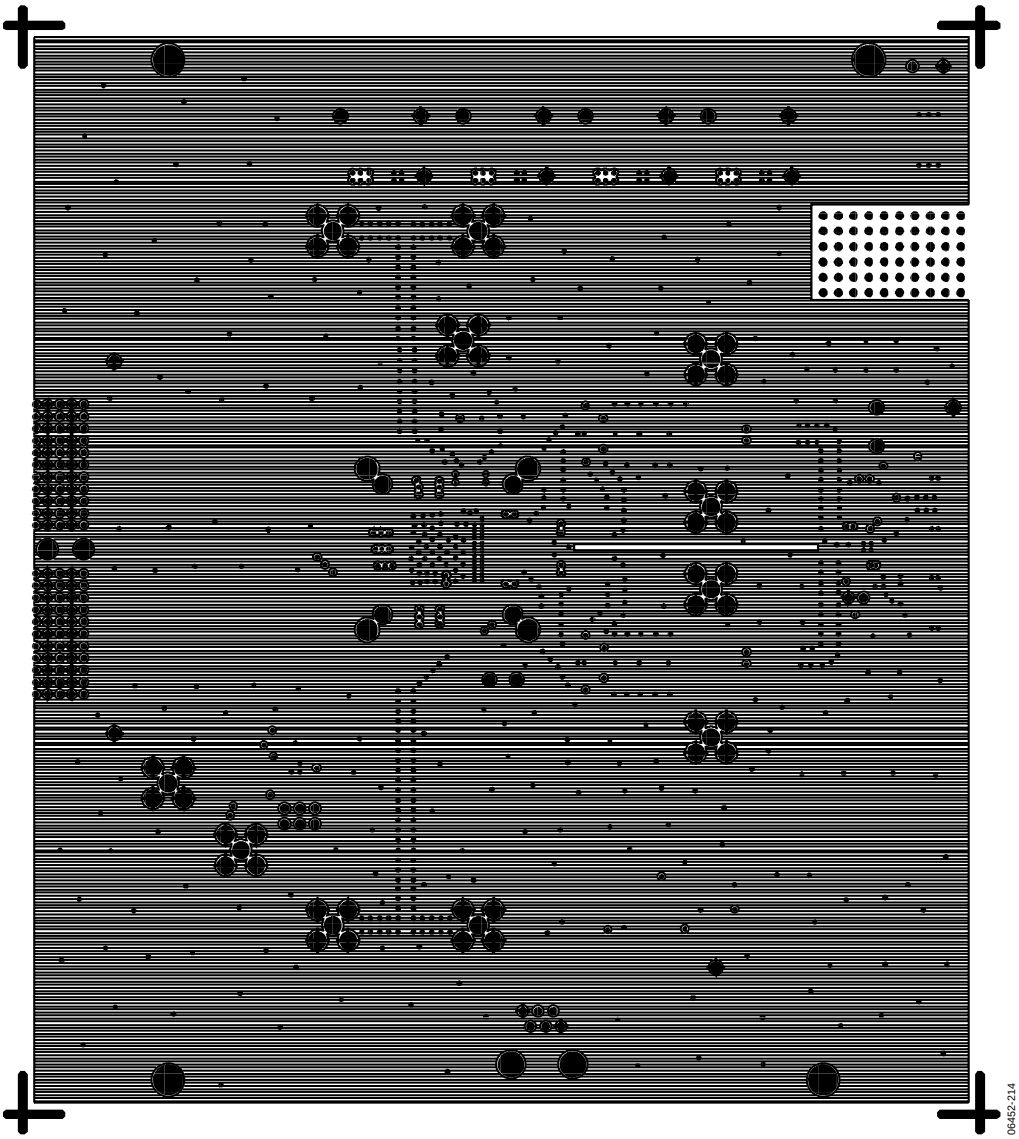


Figure 117. Evaluation Board, Rev. A, Layer 5 (Ground)

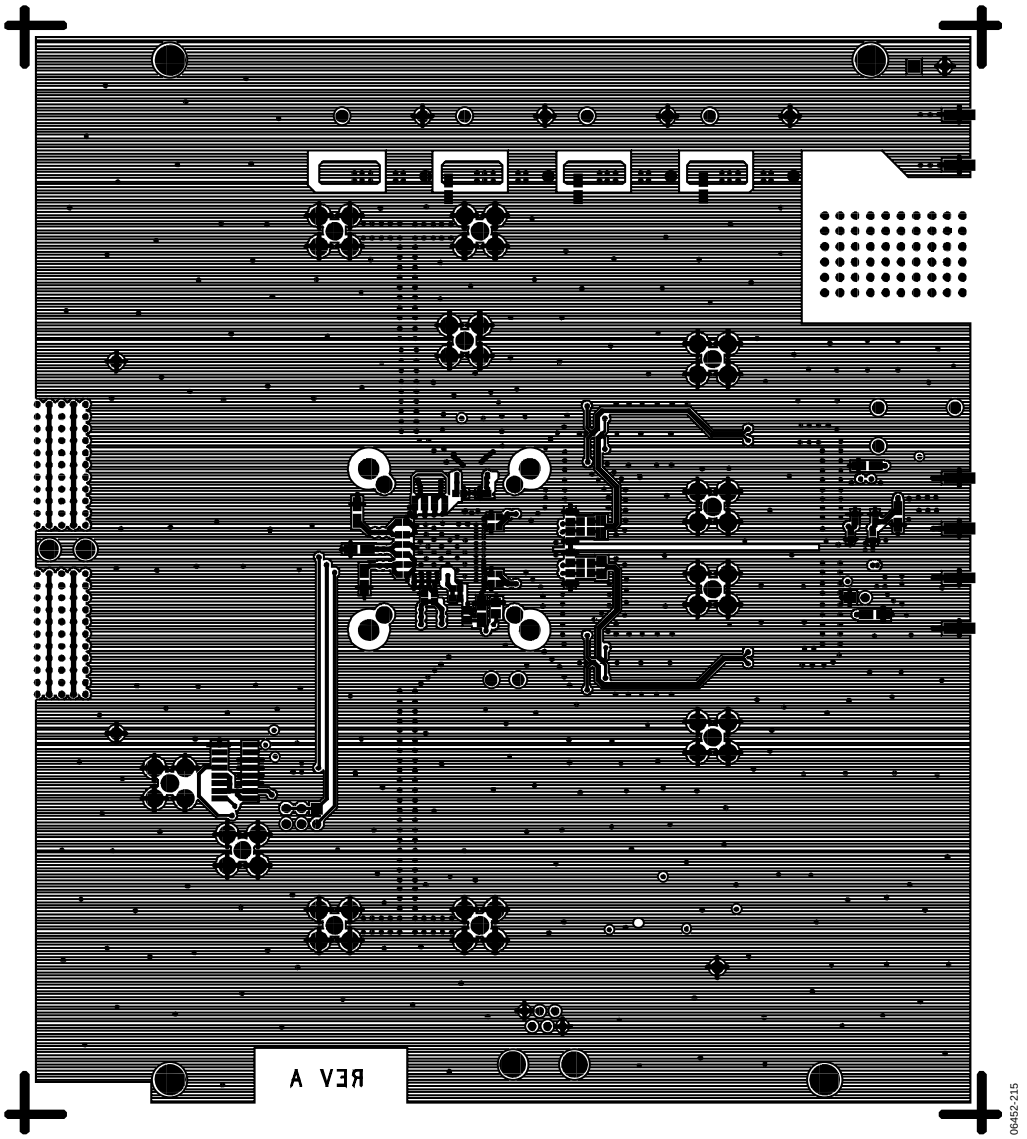


Figure 118. Evaluation Board, Rev. A, Layer 6 (Bottom)

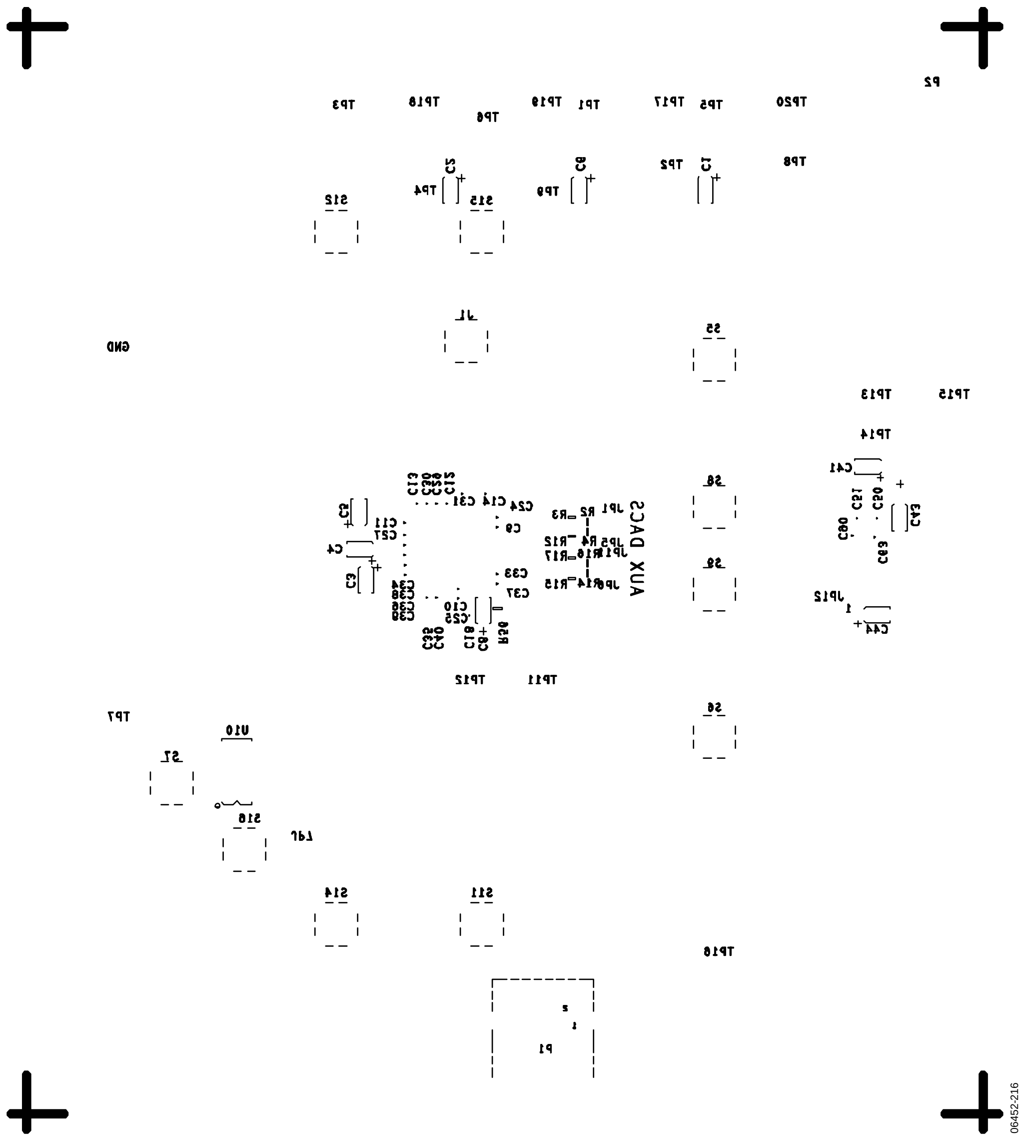
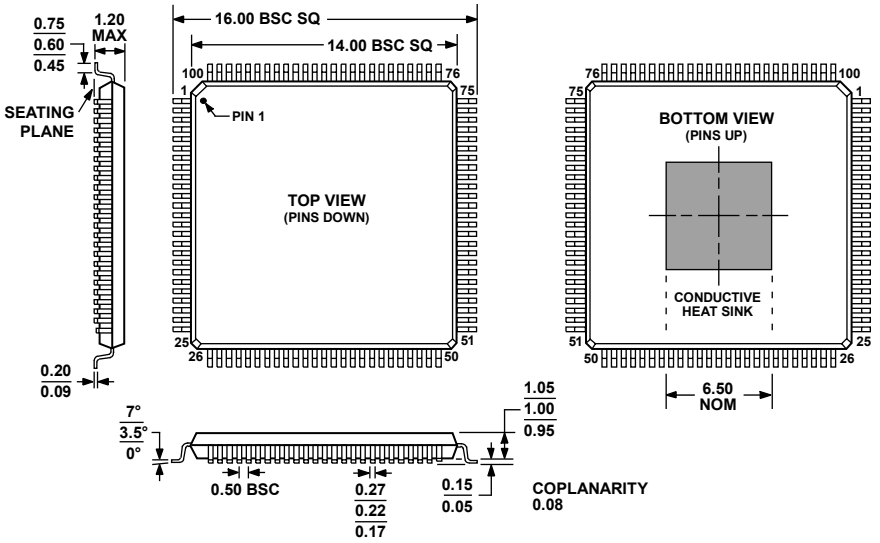


Figure 119. Evaluation Board, Rev. A, Bottom Side Silk Screen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

NOTES
1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE PACKAGE HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

040506-A

Figure 120. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9776ABSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9776ABSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9778ABSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9778ABSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9779ABSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9779ABSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9776A-EBZ[1]		Evaluation Board	
AD9778A-EBZ[1]		Evaluation Board	
AD9779A-EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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